— ST Confidential —

# *Functional Closure using the Plan-to-Closure Methodology*

*Session #1.14*

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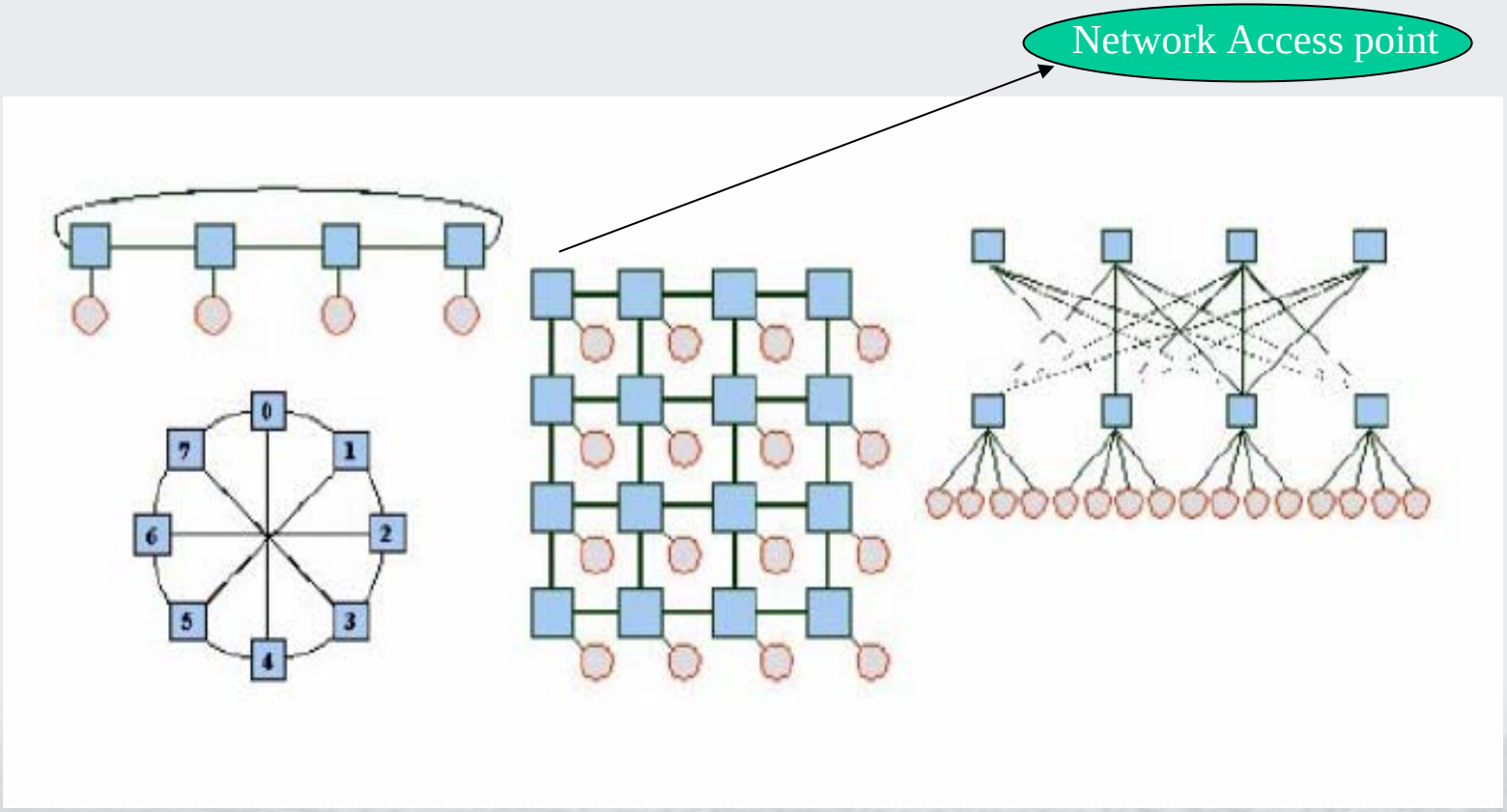
*ST Microelectronics*

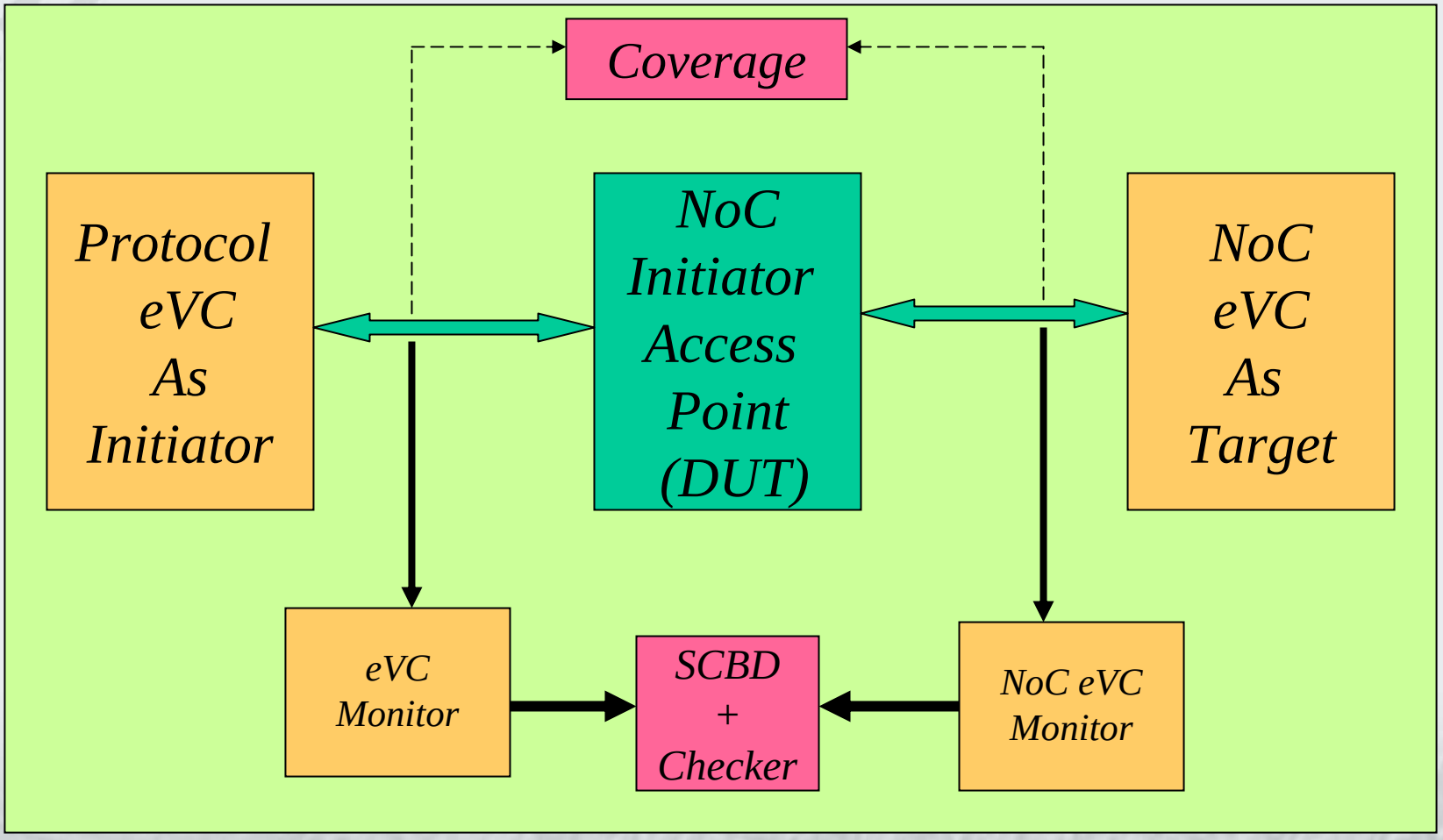
# Outline

- Overview of Network on Chip topologies
- Typical Specman Based Verification Environment
- Our Verification Strategy
  - Previous Approach
  - New Verification flow using P2C methodology
    - ✓ PLAN
    - ✓ EXECUTE
    - ✓ ANALYSIS
    - ✓ CLOSURE
- Conclusion

# *Different NoC topology*



# Specman Based Verification Env



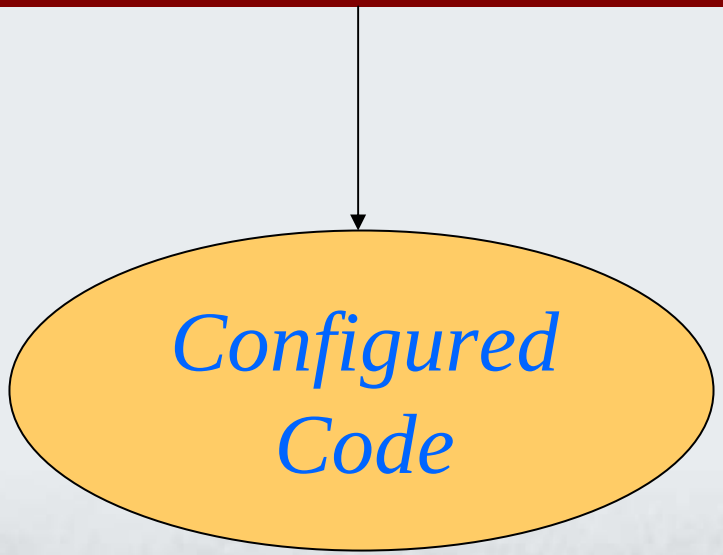
# *Previous Verification Approach*

*Without Code Coverage*

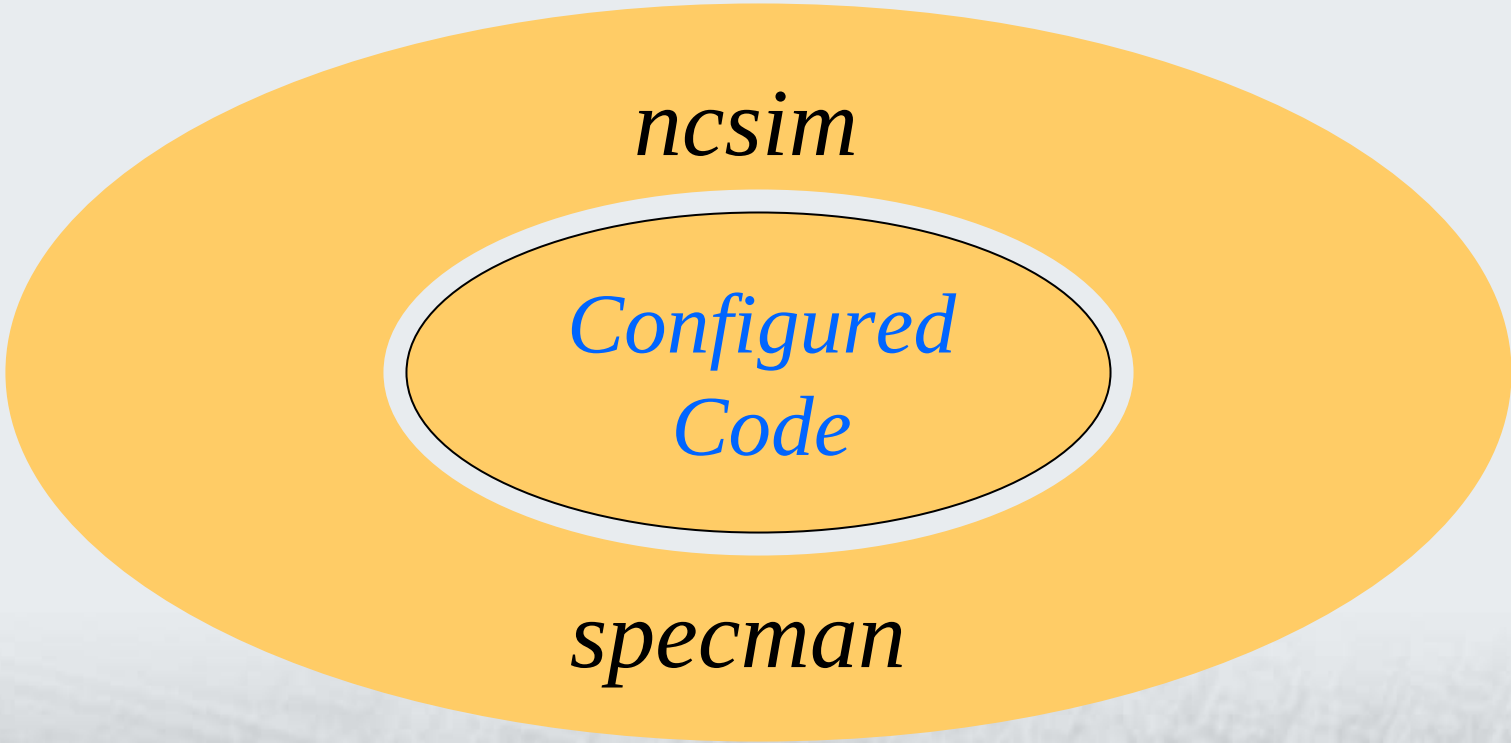
*With Code Coverage*

# *Without Code Coverage*

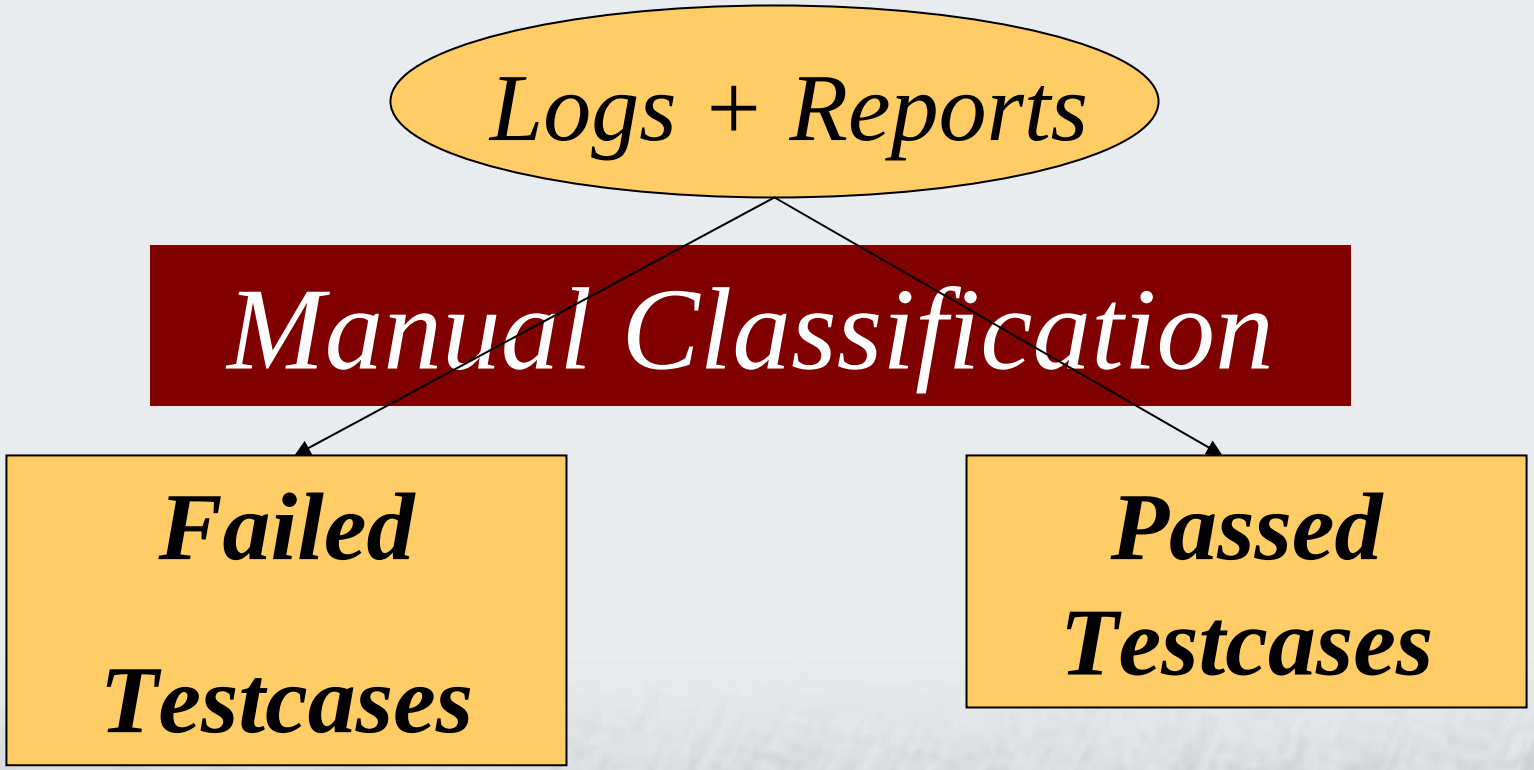
*Packaged RTL + Verification Environment + scripts*



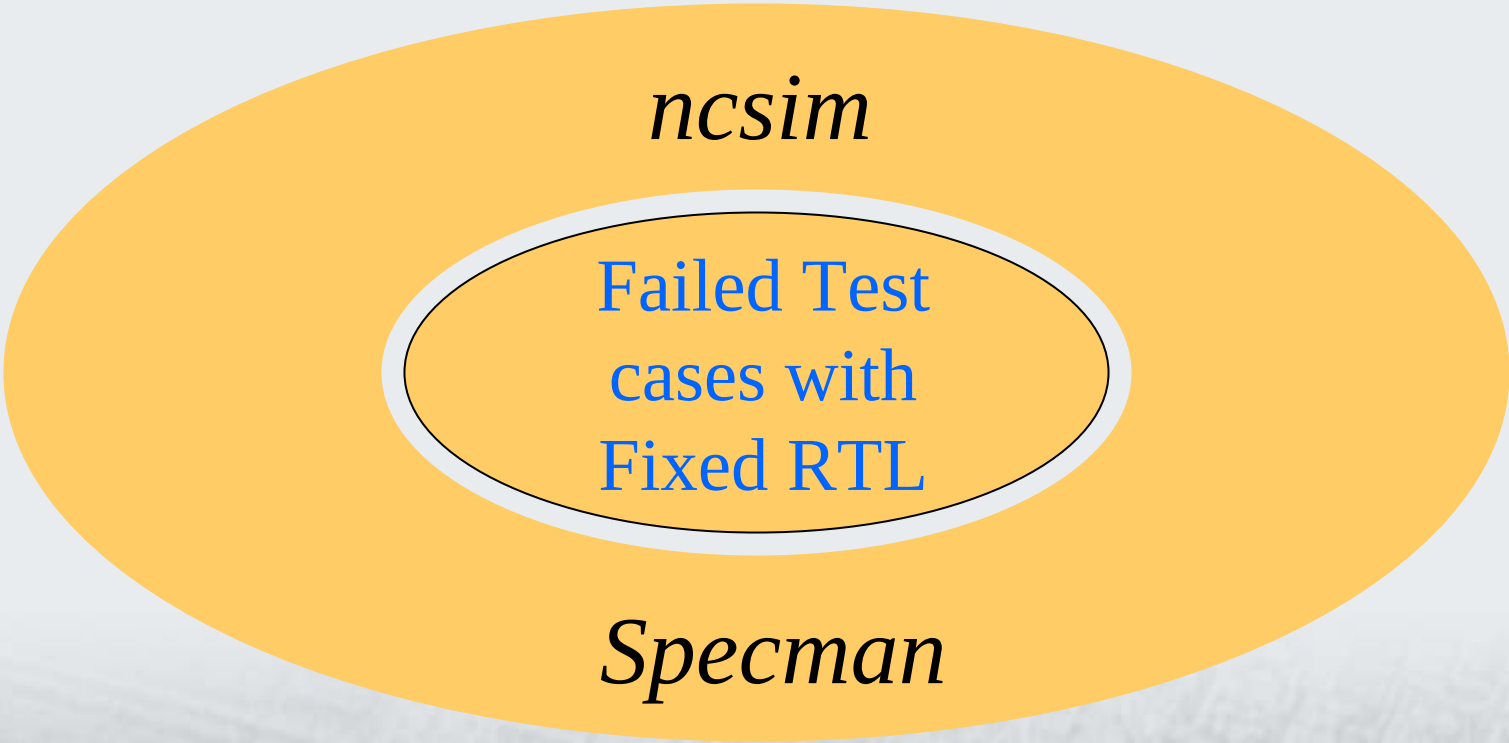
# Regression Environment



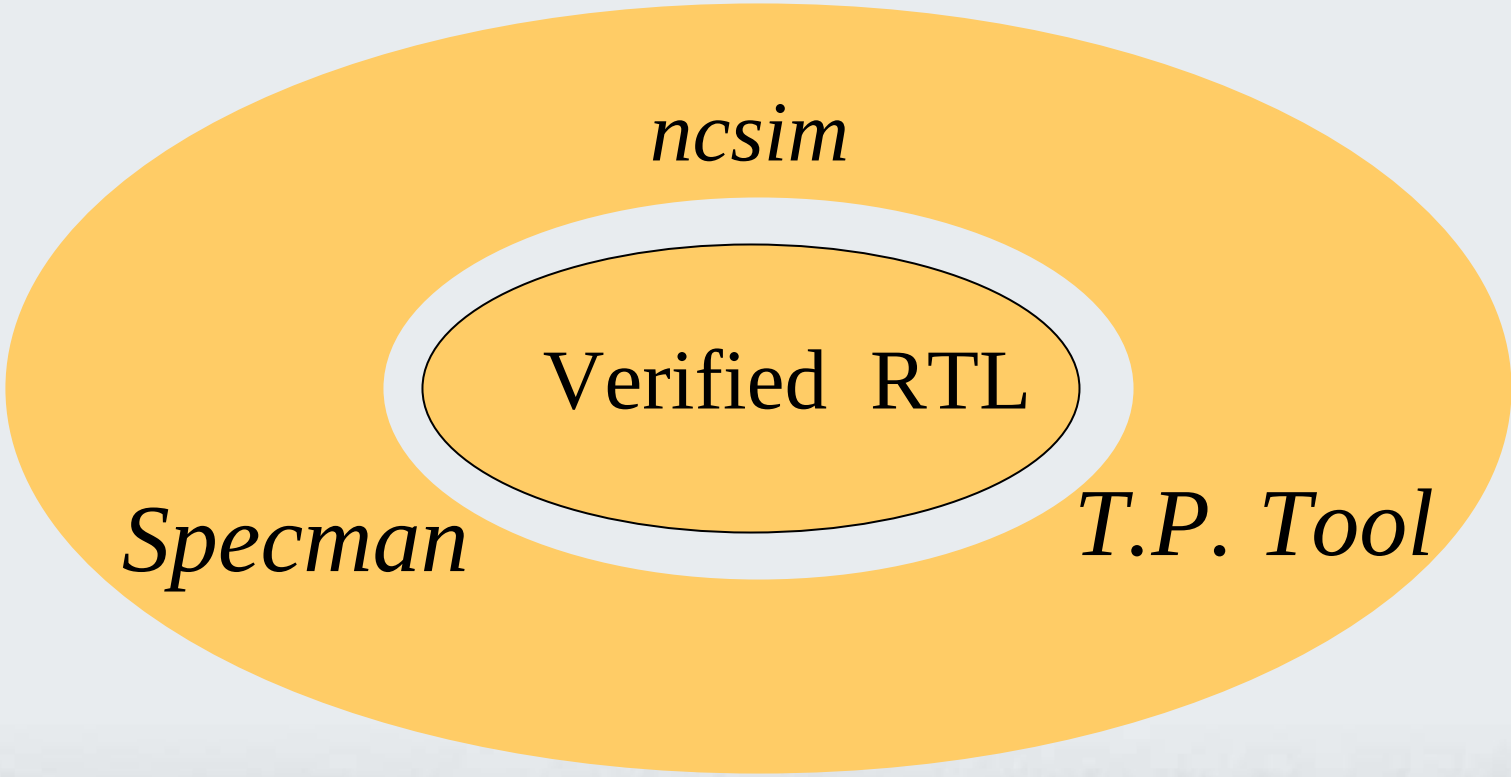
# Regression Output



# *Manual run for each failed testcase for debugging*



# *With Code Coverage*




*T.P : Third Party Tool for Code Coverage*

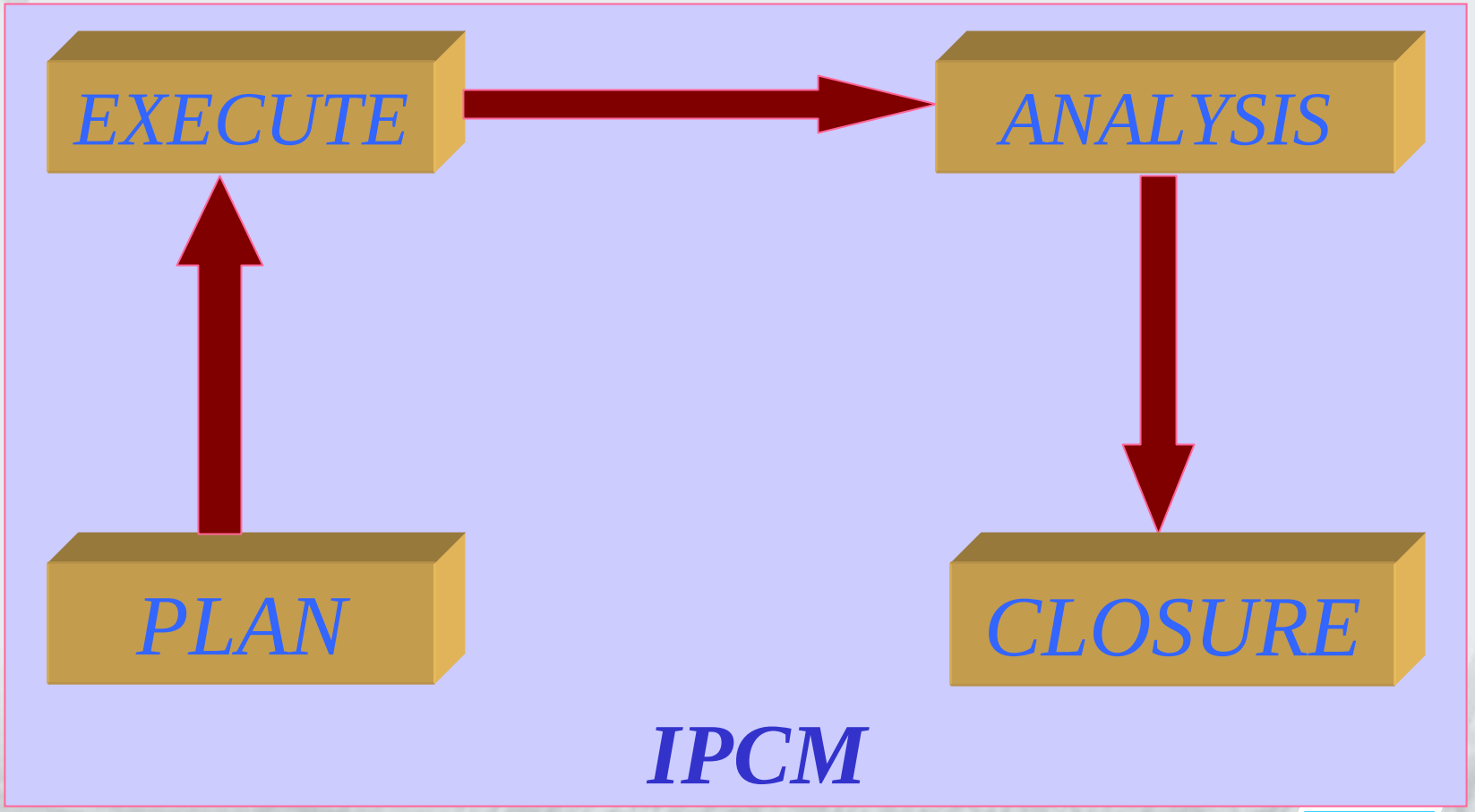
# Problems…

- Cost
  - Separate license for third party tool for code coverage
- Time
  - RTL needs separate simulation with/without code coverage
  - Simulation speed slows down by ~20-30% with third party tool used for code coverage.
  - Speed and licensing issues forced to run 2 sequential regressions
    - ✓ First to clean the design functionally (without code coverage)
    - ✓ Second to get the code coverage figures

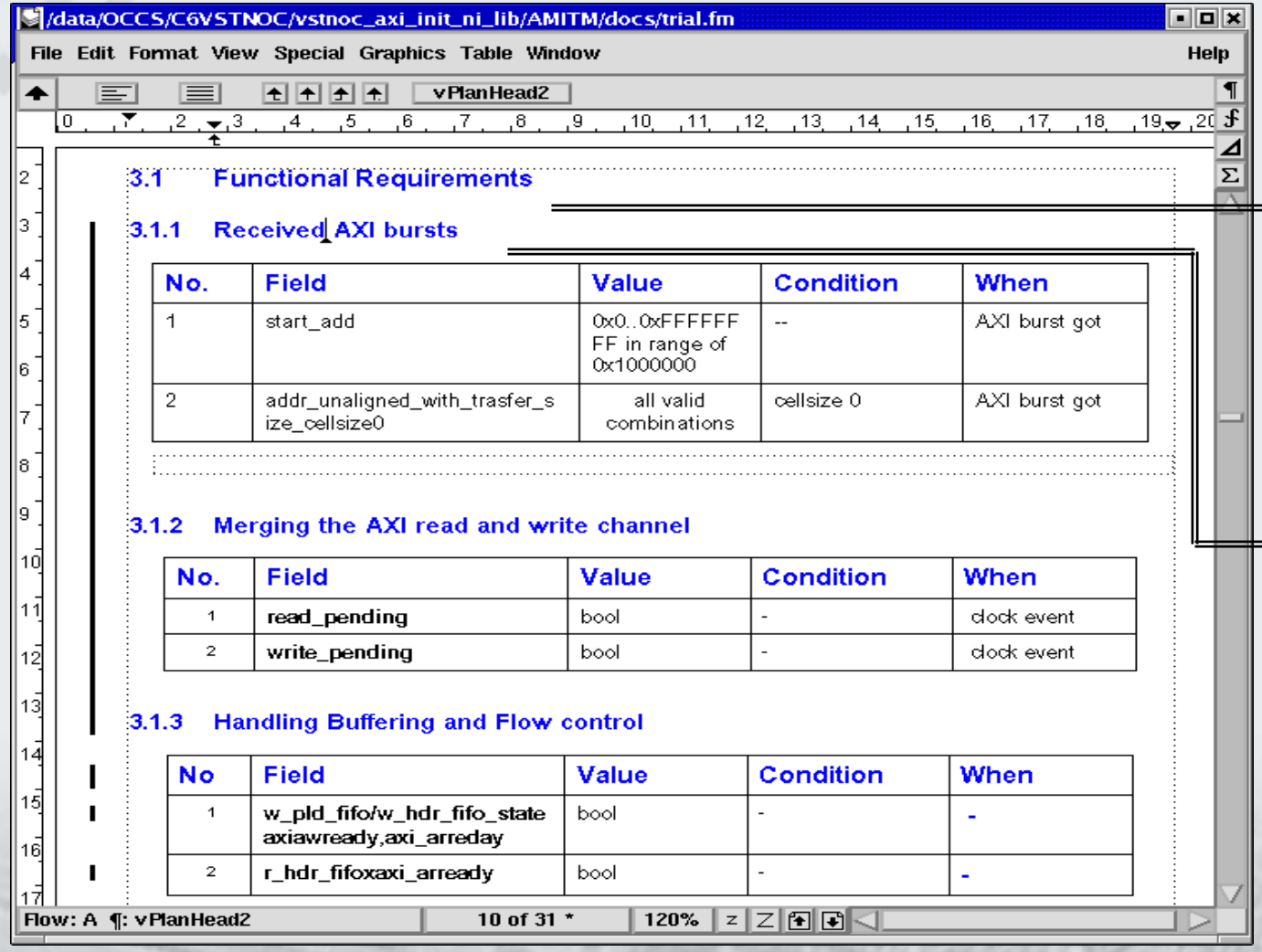
# *Problems…*

- *Debug Issues*
  - *Manual run required for failed test case.*
  - *Difficult to categorize the kind of failures.*
  - *Unable to track the progress/status of verification of IP.*

# New Verification Approach

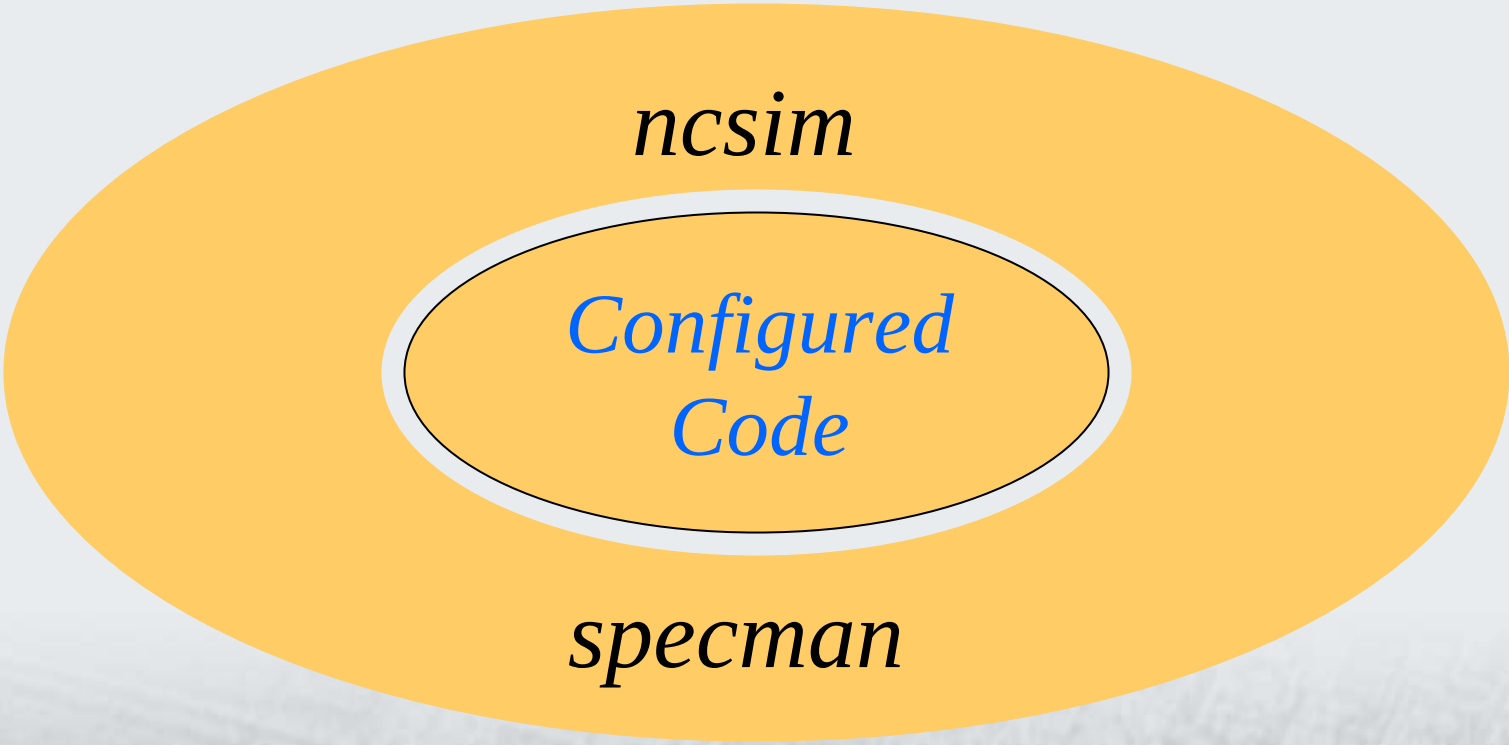


# PLAN (vPLAN)

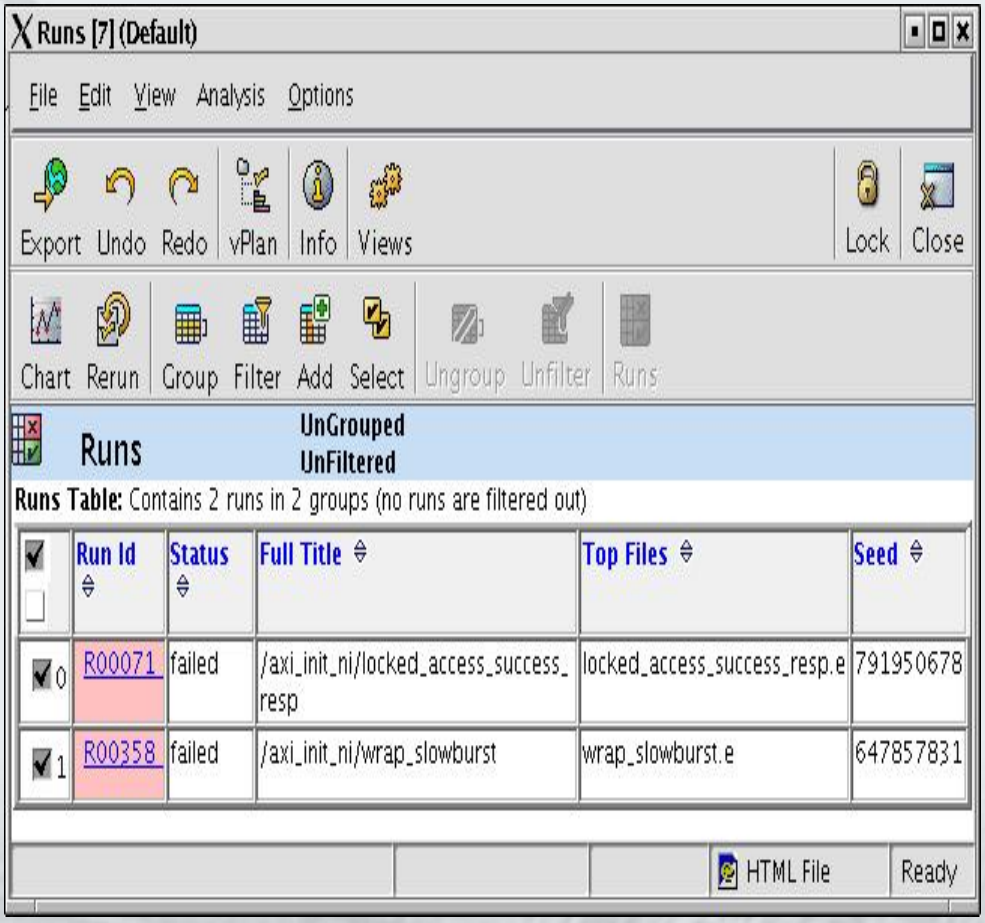

/data/OCCS/C6VSTNOC/vstnoc_axi_init_ni_lib/AMITM/docs/trial.fm
File Edit Format View Special Graphics Table Window Help
vPlanHead2
3.1 Functional Requirements
3.1.1 Received AXI bursts
No. Field Value Condition When
1 start_add 0x0..0xFFFFFFFF in range of 0x1000000 -- AXI burst got
2 addr_unaligned_with_trasfer_size_cellsize0 all valid combinations cellsize 0 AXI burst got
3.1.2 Merging the AXI read and write channel
No. Field Value Condition When
1 read_pending bool - clock event
2 write_pending bool - clock event
3.1.3 Handling Buffering and Flow control
No Field Value Condition When
1 w_pld_fifo/w_hdr_fifo_state axiawready,axi_arreday bool - -
2 r_hdr_fifoxaxi_arready bool - -
Flow: A ¶: vPlanHead2
10 of 31 *
120%

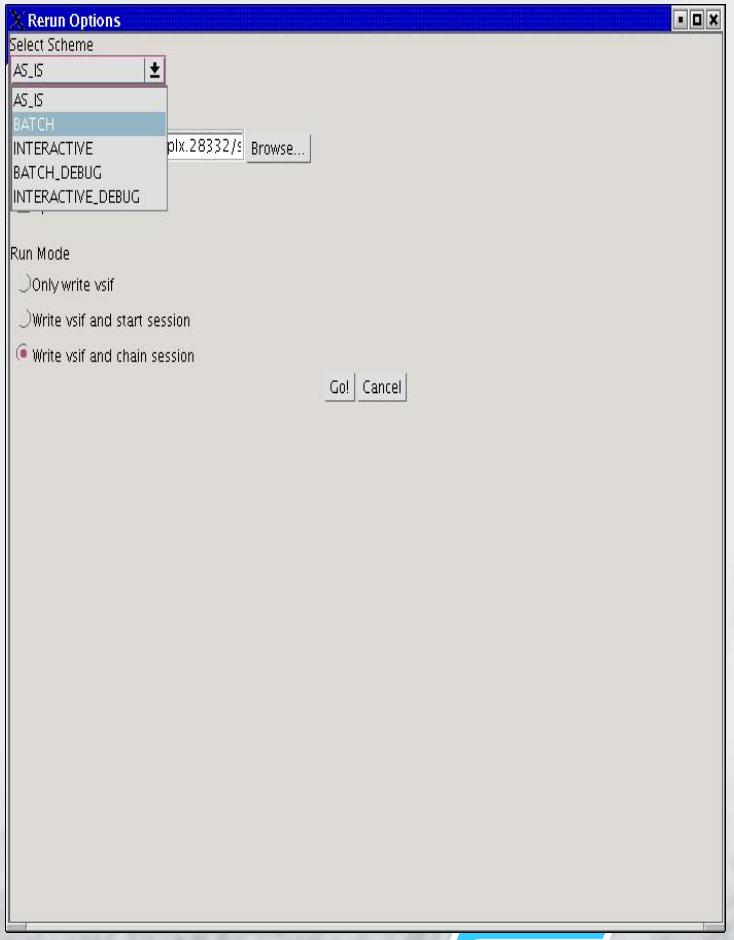

Pick formatting to apply
Required samples: vPlanAtLeast
Buckets filter: vPlanBucketsFilter
vPlan code: vPlanCode
Cover group: vPlanCoverage
Timeframe (mm/dd/yy-mm/dd/yy): vPlanDate
Details: vPlanDescription
Section goal: vPlanGoal
1 vPlanHead1
1.1 vPlanHead2
1.1.1 vPlanHead3
1.1.1.1 vPlanHead4
1.1.1.1.1 vPlanHead5
1.1.1.1.1.1 vPlanHead6
1.1.1.1.1.1.1 vPlanHead7

# *EXECUTE*

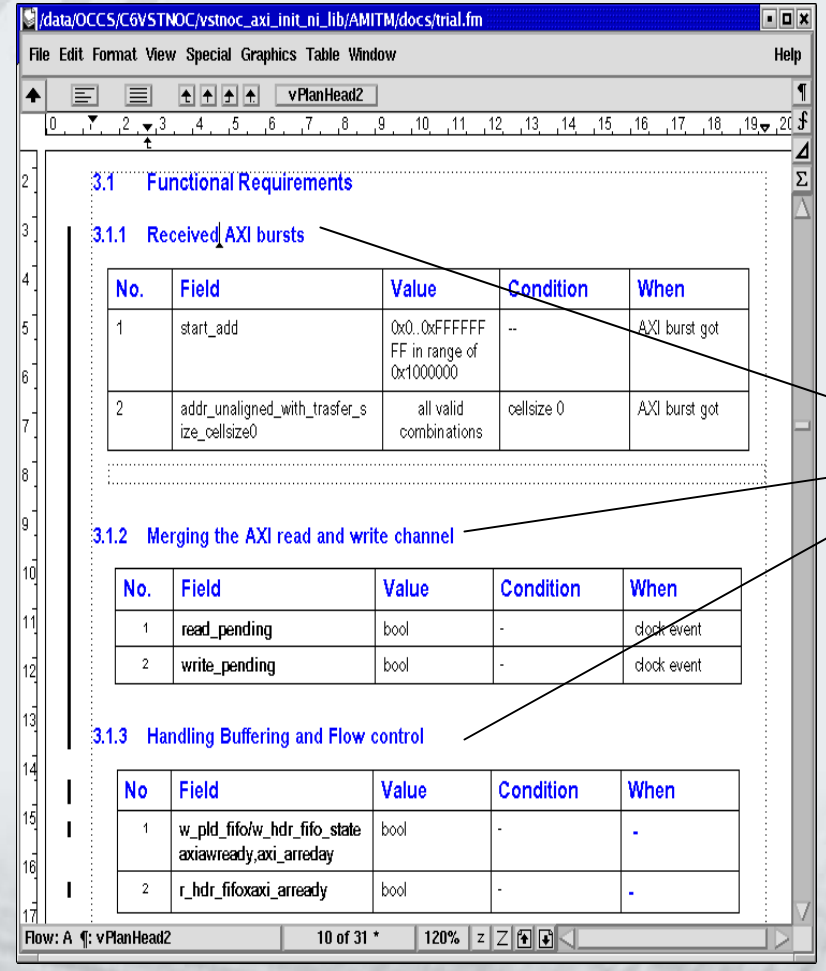


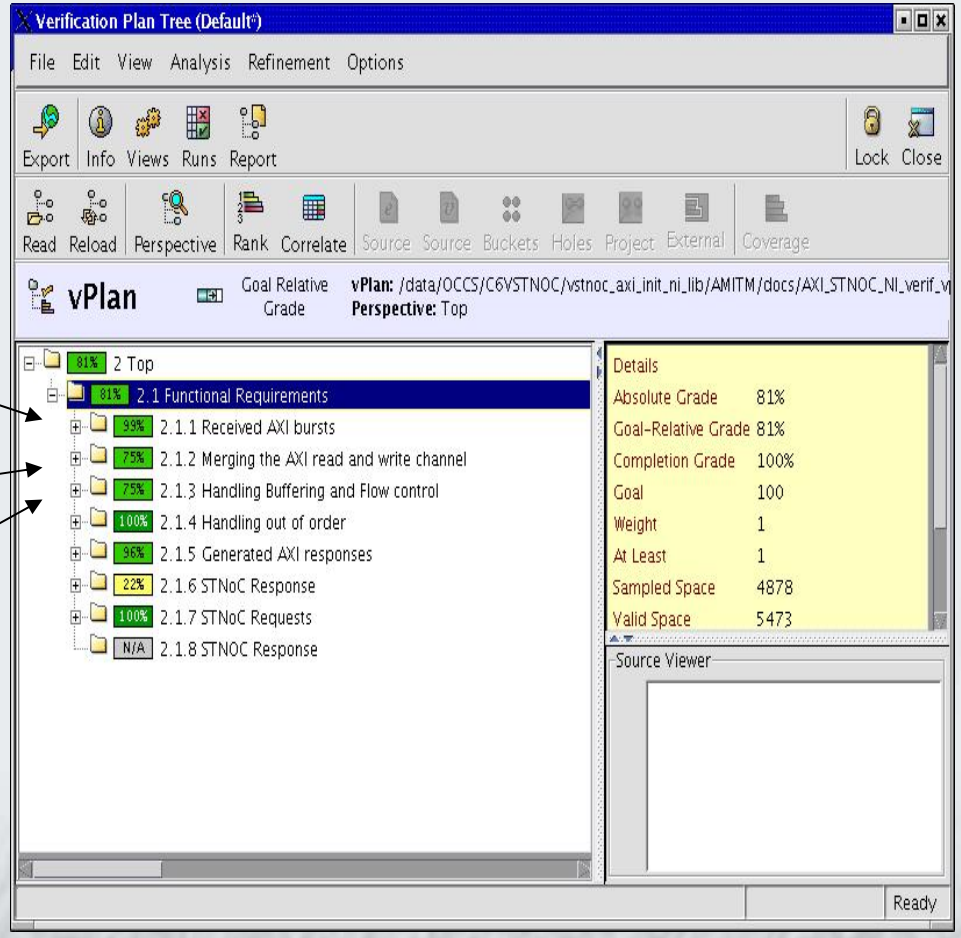
# ANALYSIS (Failures)



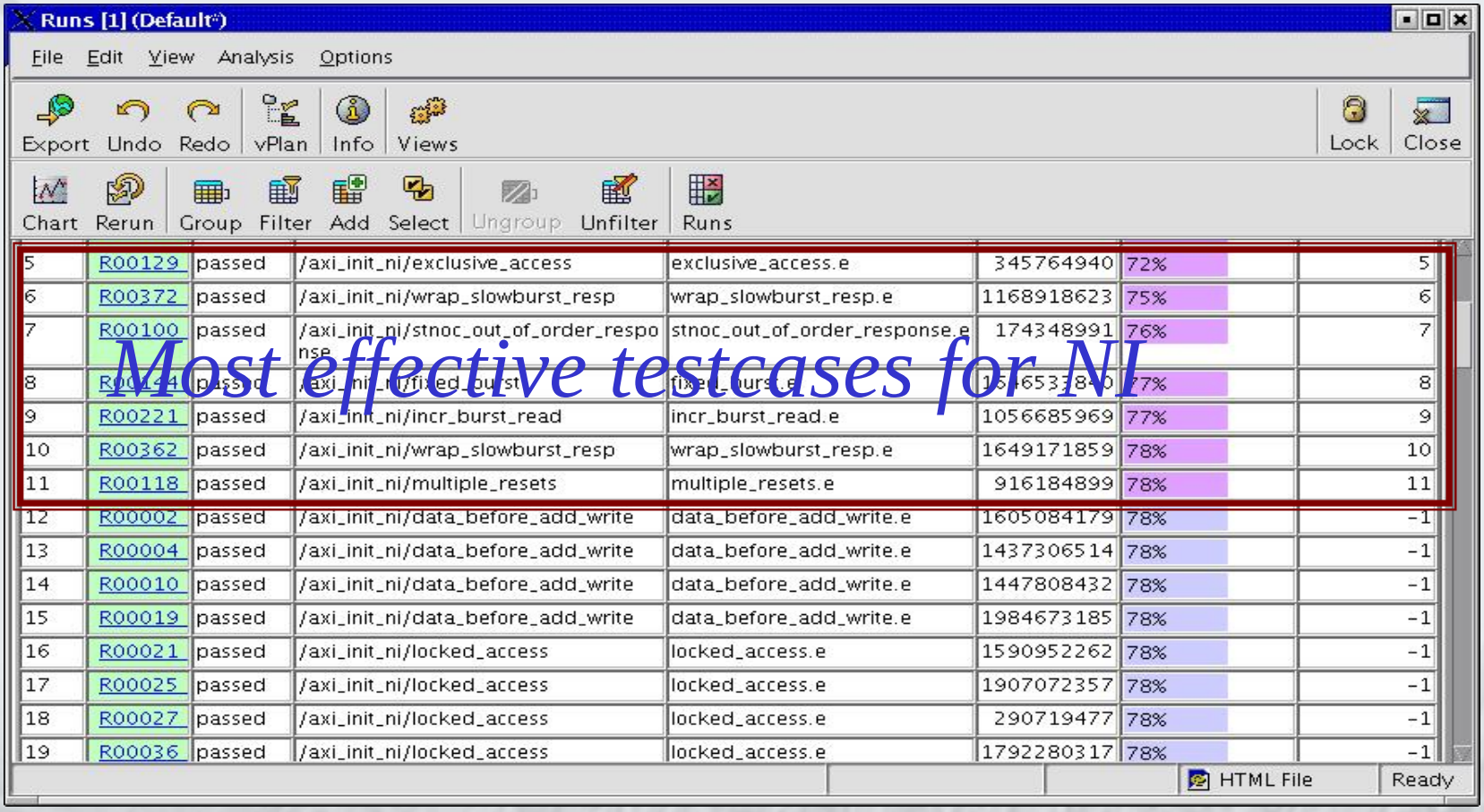



# ANALYSIS (Functional Coverage)



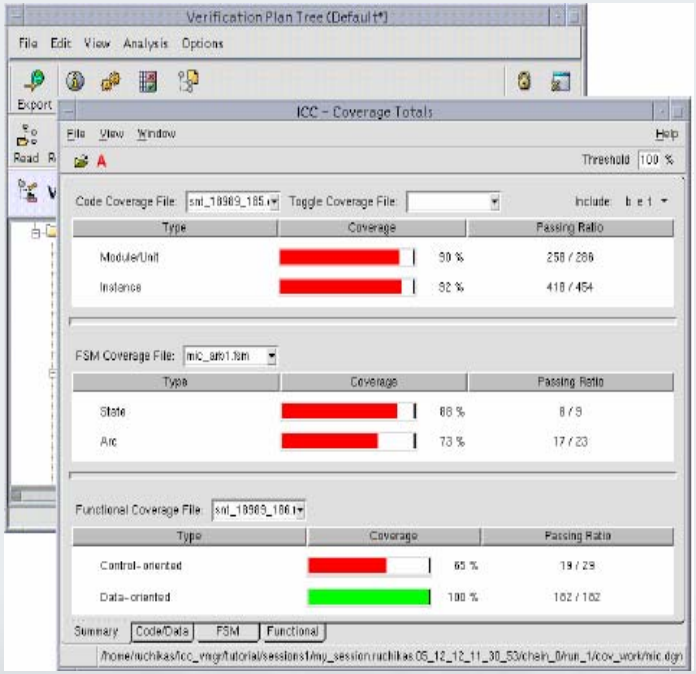



# ANALYSIS (Effective Runs)




| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 5 | R00129 | passed | /axi_init_ni/exclusive_access | exclusive_access.e | 345764940 | 72% | 5 |
| 6 | R00372 | passed | /axi_init_ni/wrap_slowburst_resp | wrap_slowburst_resp.e | 1168918623 | 75% | 6 |
| 7 | R00100 | passed | /axi_init_ni/stnoc_out_of_order_response | stnoc_out_of_order_response.e | 174348991 | 76% | 7 |
| 8 | R00144 | passed | /axi_init_ni/fixed_burst | fixed_burst.e | 1646533840 | 77% | 8 |
| 9 | R00221 | passed | /axi_init_ni/incr_burst_read | incr_burst_read.e | 1056685969 | 77% | 9 |
| 10 | R00362 | passed | /axi_init_ni/wrap_slowburst_resp | wrap_slowburst_resp.e | 1649171859 | 78% | 10 |
| 11 | R00118 | passed | /axi_init_ni/multiple_resets | multiple_resets.e | 916184899 | 78% | 11 |
| 12 | R00002 | passed | /axi_init_ni/data_before_add_write | data_before_add_write.e | 1605084179 | 78% | -1 |
| 13 | R00004 | passed | /axi_init_ni/data_before_add_write | data_before_add_write.e | 1437306514 | 78% | -1 |
| 14 | R00010 | passed | /axi_init_ni/data_before_add_write | data_before_add_write.e | 1447808432 | 78% | -1 |
| 15 | R00019 | passed | /axi_init_ni/data_before_add_write | data_before_add_write.e | 1984673185 | 78% | -1 |
| 16 | R00021 | passed | /axi_init_ni/locked_access | locked_access.e | 1590952262 | 78% | -1 |
| 17 | R00025 | passed | /axi_init_ni/locked_access | locked_access.e | 1907072357 | 78% | -1 |
| 18 | R00027 | passed | /axi_init_ni/locked_access | locked_access.e | 290719477 | 78% | -1 |
| 19 | R00036 | passed | /axi_init_ni/locked_access | locked_access.e | 1792280317 | 78% | -1 |

# ANALYSIS (Code Coverage)




*Integration between Enterprise manager and ICC enables to simultaneous view Code Coverage results.*

*Enables to view/analyze Coverage database and link it simultaneously with plan allowing to go for repetitive plan based coverage driven verification.*

# ANALYSIS (Reports for Management)

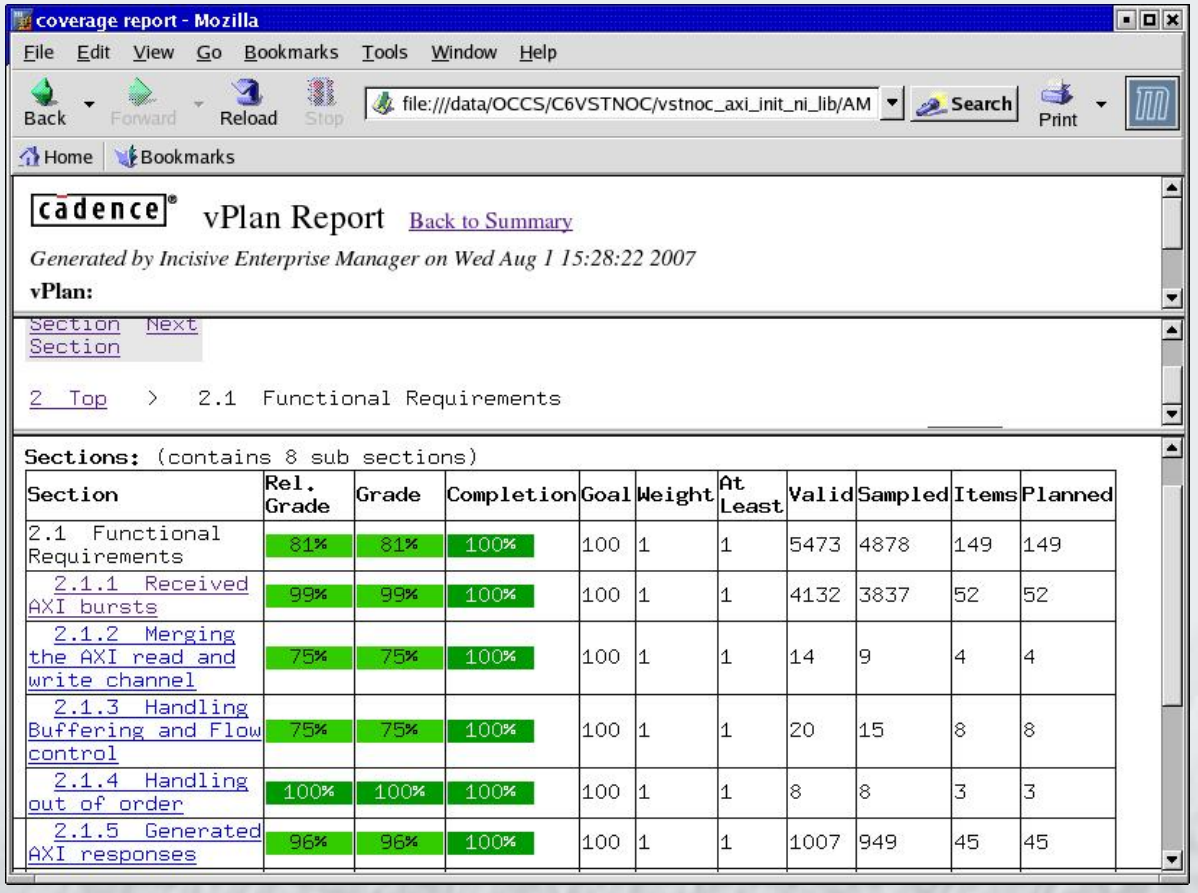
***HTML reports***

*-coverage based reports*

*-failures based reports*

*-Excellent medium to keep management updated*

*-Can keep all project members updated about the status*




| Section | Rel. Grade | Grade | Completion | Goal | Weight | At Least | Valid | Sampled | Items | Planned |
|---|---|---|---|---|---|---|---|---|---|---|
| 2.1 Functional Requirements | 81% | 81% | 100% | 100 | 1 | 1 | 5473 | 4878 | 149 | 149 |
| 2.1.1 Received AXI bursts | 99% | 99% | 100% | 100 | 1 | 1 | 4132 | 3837 | 52 | 52 |
| 2.1.2 Merging the AXI read and write channel | 75% | 75% | 100% | 100 | 1 | 1 | 14 | 9 | 4 | 4 |
| 2.1.3 Handling Buffering and Flow control | 75% | 75% | 100% | 100 | 1 | 1 | 20 | 15 | 8 | 8 |
| 2.1.4 Handling out of order | 100% | 100% | 100% | 100 | 1 | 1 | 8 | 8 | 3 | 3 |
| 2.1.5 Generated AXI responses | 96% | 96% | 100% | 100 | 1 | 1 | 1007 | 949 | 45 | 45 |

# *CLOSURE*

- *Functional Coverage metrics available*
- *Code Coverage Metrics available*
- *Assertion Metrics, if used available*

# Advantages (IPCM)

- *eManager benefits in verification process automation*
- *Manages and deploys thousands of simulations, thus shortens the overall verification cycle*
- *Reduces overall debug time*
- *Ensures better quality of IP, due to plan driven coverage based verification*

# *Conclusion…*

- *Efficient failure analysis capabilities help reduce Verification cycle of IP thus help improve time to market.*
- *Plan driven Coverage based verification ensure high degree of quality of IP.*
- *Tight integration between simulator (ncsim) & generator (specman) & coverage engine (ICC/ specman) enables faster path towards closure.*

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# CONNECT: IDEAS

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