# cādence<sup>®</sup>

# Cadence System Development Suite

Open, connected, and scalable platforms to speed hardware/software development

The Cadence<sup>®</sup> System Development Suite accelerates the system integration, validation, and bring-up process with a set of four platforms for concurrent hardware/software design and verification. It supports industry standards and multiple levels of design abstraction, it allows easy migration among platforms and between hardware/software domains, and it can scale to meet performance, capacity, and software distribution volume needs as they change. Using the System Development Suite, design teams can shorten system integration time by up to 50%.

### System Development Suite

The Cadence System Development Suite provides an open, connected, and scalable set of hardware/software development platforms that spans the entire design cycle, from architectural-level software development to post-RTL prototyping.

Built on top of market-leading Cadence technologies—the Incisive® Verification Platform and the Palladium® XP Verification Computing Platform—the System Development Suite extends the power of familiar simulation and emulation-based environments with two new hardwareaware software development platforms: the Cadence Virtual System Platform and the Cadence Rapid Prototyping Platform.

Each of the four platforms is optimized for a different part of the system development flow.



Figure 1: A comprehensive solution for faster, more predictable, and more profitable system development

#### Virtual System Platform

A virtual prototyping solution that automates modeling, speeds HW/SW debugging, and connects tightly to RTL and testbench simulation—ideal for software development at the architecture and prototype design phases.

#### Incisive Verification Platform

A comprehensive solution for verification planning and management, verification IP creation and reuse, testbench simulation, mixed-signal simulation, and formal analysis—ideal for block- and chip-level verification.

#### Verification Computing Platform

A unified environment for advanced simulation acceleration and emulation, with hot-swap capability for instant migration among tasks, plus HW/SW co-verification with dynamic power analysis—ideal for system validation.

#### **Rapid Prototyping Platform**

An FPGA-based prototyping solution that speeds bring-up time and combines high-capacity FPGA boards with a complete implementation and debug software flow—ideal for exhaustive regression tests and cycleaccurate software development.

## **Benefits**

- Minimizes risk, reduces costs, and speeds time to market by greatly accelerating system integration, validation, and bring-up
- Offers scalable performance with functionality tradeoff, allowing hardware developers to use a standards-based metric-driven verification flow (with acceleration)
- Allows designers to run and debug their software on top of a representation of the hardware platform very early in the process
- Leverages in-circuit emulation to help designers quickly bring-up and validate the full system
- Enables exhaustive regression runs and cycle-accurate, high-performance, pre-silicon software development
- Allows system architects to quickly build virtual platforms using standard transaction-level models (TLMs), then simulate and analyze them with their legacy RTL code, and transparently interact with software developers
- Shortens system integration time by up to 50%



Figure 2: Only Cadence delivers an open, connected, and scalable continuum of system development platforms



Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com

© 2011 Cadence Design Systems, Inc. All rights reserved. Cadence, the Cadence logo, Incisive, Palladium, and SpeedBridge are registered trademarks of Cadence Design Systems, Inc. All others are properties of their respective holders. 22061 04/11 MK/DM/PDF