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LSI Corporation and Cadence

"At the end of the day, it's all about increasing the competitiveness of our products. With a strong mixed-signal verification process based on Cadence technologies, we can make more improvements with less iteration. This enables us to get to market faster."

Hao Fang, Design Manager, LSI Corporation

LSI Corporation provides custom and standard product integrated circuits (ICs), adapters, and software for the storage and networking markets. The company's storage products include new innovations such as solid-state storage and 6Gb/s serial attached SCSI (SAS) switches. LSI's system-on-chip (SoC) solutions power hard disk drives and solid-state drives, enabling higher capacity points to accommodate ever-increasing amounts of data. The LSI portfolio for wireless, enterprise, and wireline networking allows intelligence, control, and security to be distributed throughout the network.

The Challenge

When the LSI Storage Peripheral Division (SPD) Group began work on its next-generation SoC, it needed a reliable, thorough way to verify its large analog intellectual property (IP) components.

"We had a highly effective universal method for digital, but our approach to analog was more manual and ad hoc," explains Hao Fang, Design Manager, SPD Group, LSI Corporation. "Our analog verification process lacked the same level of coverage or quality control. We needed to improve it to meet the stringent requirements of our IP delivery."

Customized for optimal performance and cost, LSI SoCs support high data rates with best-in-class system performance at the lowest power. LSI offers a wide range of programmable parameters in each SoC to enable fast time to market and maximum drive-assembly yield.

"Our main verification goal for our mixed-signal designs was to provide a higher-quality product in the shortest possible timeframe," Fang says. "We don't want our chips to come back and require debug. We want to get it right the first time."

Business Challenges

- Establish a proven mixed-signal methodology to verify analog IP for a mixed-signal chip
- Produce a high-quality product in a short time-to-market window

Design Challenges

- Upgrade ad-hoc, manual verification methodology for analog IP
- Leverage current, optimal verification flow for digital IP

Cadence Solutions

- Incisive Enterprise Simulator
- Incisive Enterprise Manager
- Incisive Enterprise Specman Elite Testbench
- Virtuoso AMS Designer
- Virtuoso Schematic Editor
- Virtuoso Analog Design Environment
- Customer Support

Results

- Established a methodology that can be extended to analog verification
- Expanded analog design verification coverage and improved product quality
- Met design and performance specifications

The Solution

To bring its analog verification process up to par with its digital verification process, LSI decided to deploy the Universal Verification Methodology (UVM), a standard developed by Accellera to foster universal verification IP (VIP) interoperability as the basis for mixed-signal verification. The UVM is widely being used by digital verification engineers to address their most complex verification challenges. LSI extended the UVM to include verification planning for analog blocks, checking, and assertion techniques, as well as analyzing analog functional coverage, to apply the metric-driven verification approach to mixed-signal verification.

Virtuoso technology meets analog verification needs

LSI's SPD Group recognized the need for a new analog verification methodology for the mixed-signal chip and began looking into several options. Fang's team decided that Cadence offered the complete toolset for a consistent mixed-signal methodology across the product's analog and digital IP blocks. The other deciding factor was the long collaboration and success between the two companies.

According to Fang, the Cadence® Virtuoso® unified custom/analog flow provided the right fit for LSI's analog verification methodology. Specifically, the company used Virtuoso AMS Designer, Virtuoso Schematic Editor, Virtuoso Analog Design Environment, and Virtuoso Layout Suite. For many years, LSI has also used Cadence Incisive® Enterprise Simulator, Incisive Enterprise Manager, and Incisive Enterprise Specman Elite® Testbench to verify some digital IP blocks. Because Incisive Enterprise Simulator supports the UVM, LSI engineers can quickly and easily integrate it with their analog verification flow.

"With Cadence technology, we can improve verification coverage to catch more errors earlier in the process compared to our previous ad-hoc, manual verification process."

"First we created a prototype to see what we could accomplish using Cadence technologies and the UVM standard for our analog verification needs," Fang says. "Cadence provided models for the analog IP blocks and helped us create easy interchangeability between our digital and analog flows. It was very easy for us to do mixed-mode simulations because everything was contained in the same environment. And we were able to accomplish all this with increased automation, which saves valuable time."

The result of the new mixed-signal flow is a more predictable schedule and the ability to detect and correct errors early. This is far less costly than fixing them after the product is released.

"With Cadence technology, we can improve verification coverage to catch more errors earlier in the process compared to our previous ad-hoc, manual verification process," Fang says.

Reliable and knowledgeable customer support

According to Fang, the expertise offered through Cadence Customer Support was a key benefit. Cadence helped LSI bridge the knowledge gap between analog design and verification methodology. This partnership enabled LSI to work through challenges and realize a complete, integrated verification solution.

"The Cadence support team worked with us to understand what was needed and to create solutions for the new methodology," he says. "This helped us understand each other and reach for common goals. Cadence has been good at responding and providing solutions in a timely fashion. Overall I'm very happy with the expertise they provide."

Looking ahead

Cadence helped to create detailed modules and specific tests to meet LSI's unique verification needs. Together the companies have developed an infrastructure that's expandable and portable for future efforts.

"During this project we proved to ourselves that digital concepts can be applied to analog," Fang says. "Our methodology doesn't solve every analog/mixed-signal problem, but it can solve the majority of them."

Using the UVM and a metric-driven approach, LSI's new verification process is highly reconfigurable and useable as the company moves forward on new projects. For example, Fang's team is now using the methodology for a preamplifier product.

Summary

With Cadence mixed-signal solutions and the UVM, LSI was able to leverage its digital verification process into the analog arena to save time and improve quality. By running more simulations on analog blocks with better coverage, the SPD Group has gained better predictability and the confidence that it will deliver a chip with first-time success.

"At the end of the day, it's all about increasing the competitiveness of our products," Fang says. "With a strong analog verification process based on Cadence technologies, we can make more improvements with less iteration. This enables us to get to market faster."

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