cādence®

Cadence Coherency Verification Solution

For more than 10 years, Cadence has been the leading provider of verification IP (VIP) for the ARM® AMBA® protocol family, including the latest AMBA 4 specifications. Now Cadence offers the industry's first complete solution for cache coherency verification. By combining Cadence® VIP for the ACE™ protocol with an Interconnect Monitor and the Compliance Management System, Cadence provides engineers with the all the tools needed to ensure full SoC and system-level design coherency.

The Cache Coherency Challenge

Today's most popular mobile devices rely on multiple processors, such as the ARM Cortex™ A15, to satisfy consumer demand for high performance and respon-siveness. But a software-based approach to cache coherency takes too many cycles and consumes too much power. To optimize performance and battery life, ARM introduced the AXI™ Coherency Extensions (ACE) protocol, which provides hardware-based cache coherency.

While this is good news for consumers, verifying cache-coherent SoCs and systems that employ the ACE protocol introduces new challenges for engineers. They need to ensure coherency (i.e., that only up-to-date data is used). Traditional directed test–style verification schemes are not up to the task because of the huge range of scenarios and checks needed to validate coherency. Engineers now need specialized verification tools that not only ensure ACE compliance, but also ensure that the design is coherent.

The Cadence Coherency Verification Solution

Cadence provides the industry's first complete solution for cache coherency verification. It comprises three key technologies that enable you to verify both ACE compliance and end-to-end design coherency.

Cadence VIP for the ACE protocol: constrained-random stimulus generation to mimic all possible scenarios and checks to ensure protocol compliance

Interconnect Monitor: protocol compliance checking including system coherency checks at the inter-connect level
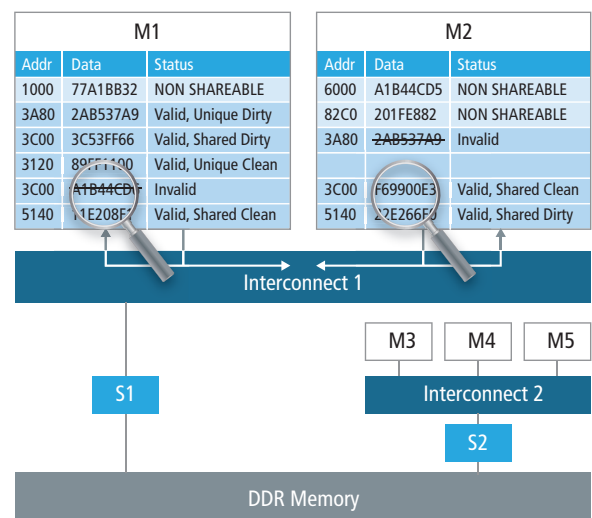

Figure 1: Verifying cache coherency is challenging

Compliance Management System: a coverage map, a verification plan, and pre-defined stimulus to achieve high coverage without test writing

Benefits

- Creates the scenarios necessary to mimic processor and memory behavior including snooping operations

- Ensures end-to-end data coherency (i.e., ensuring that only valid data is used)

- Correctly manages all simultaneous write/snoop combinations

- Ensures that no scenarios create deadlocks

- Leverages a metric-driven verification methodology
- Supports all leading simulators, verification methodologies (UVM/OVM, VMM), and verification languages (SystemVerilog, *e*)
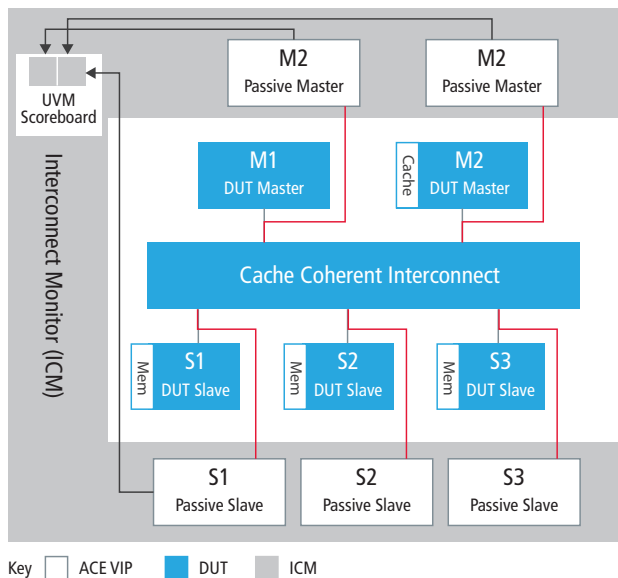

Key ☐ ACE VIP ■ DUT ■ ICM

Figure 2: Cadence provides a complete coherency verification solution that stimulates and monitors to ensure protocol compliance and interconnect behavior

Features

Cadence AMBA Verification IP (VIP)

Proven on more than 2,000 designs, Cadence VIP provides you with hundreds of protocol scenarios and the coverage needed to ensure that you are fully compliant with AMBA 4 specifications. Using Cadence VIP relieves you of creating the scenarios that you can think of and, perhaps more importantly, those that you did not think of.

Cadence VIP for the ACE protocol provides constrained-random test generation and functional coverage to verify the operation of masters and slaves. It ensures that each individual processor and memory behaves correctly.

Interconnect Monitor (ICM)

The Cadence ICM checks data integrity among all the ports on the interconnect. It monitors the interconnect to ensure that communication between all components is accurate and in compliance with the ACE specification. The ICM is also extendable and customizable to enable design-specific checking, such as support for all bus-oriented protocols.

Active Master	Passive Master
- Sends read/write transactions using AXI 4 channels - Receives and responds to snoops - Keeps its cache updated according to current conditions	- Checks full AXI 4 protocol correctness - Checks cache responses and cache coherency - Checks transaction attributes to ensure alignment with domains - Checks barrier transaction correctness
Active Slave	Passive Slave
- Sends read/write transactions - Models sparse memory modules - Provides fake snoop transactions if needed	- Checks AXI 4 protocol correctness - Checks snoop transactions - Checks transaction responses

Figure 3: Example checks provided by Cadence VIP

Compliance Management System (CMS)

The Cadence CMS provides two key functional capabilities. The first is an ACE-specific verification plan (vPlan). The vPlan, an executable document, maps the necessary coverage and checks directly to the ACE specification. The second is an extensive compliance test suite that yields a high level of functional coverage—typically in excess of 90% for an ACE master.

Both the vPlan and the compliance test suite are organized modularly. This enables parts of the specification not in use to be excluded, allowing you to focus on the greatest risk areas.

Figure 4: An ACE vPlan maps the necessary coverage and checks directly to the ACE specification

More information regarding the Cadence VIP Catalog is available at: http://www.cadence.com/products/fv/verification_ip.

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Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. **www.cadence.com**