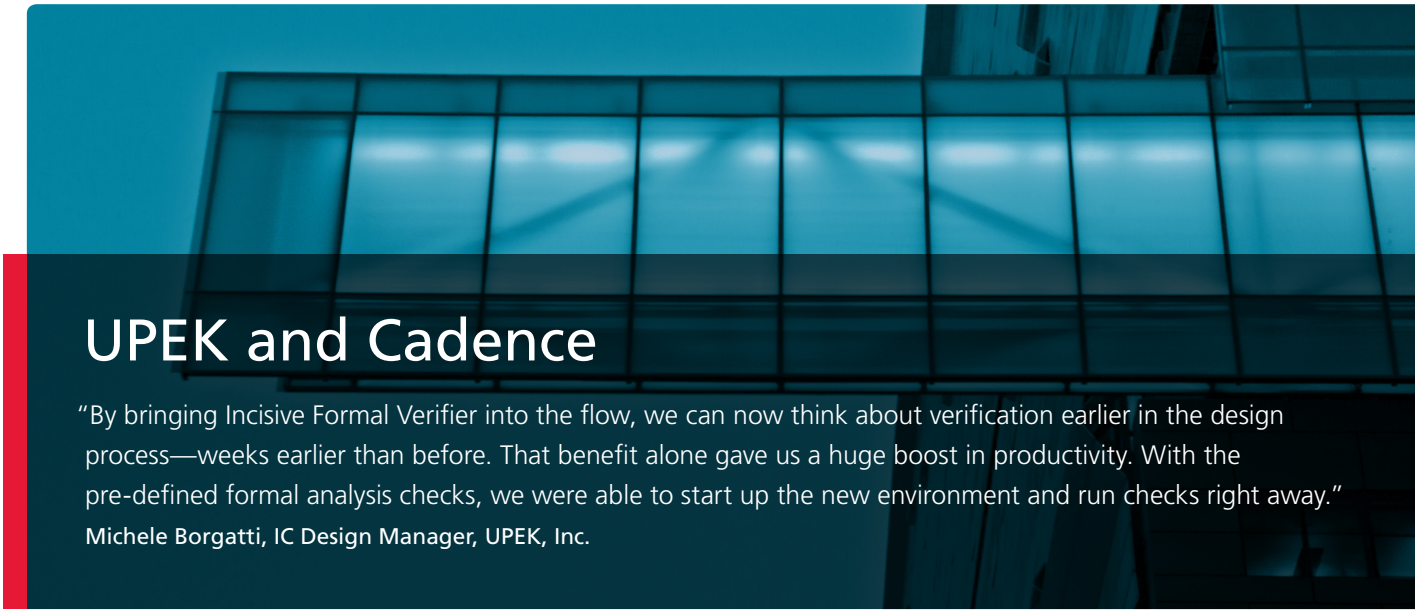
cadence®



UPEK and Cadence

"By bringing Incisive Formal Verifier into the flow, we can now think about verification earlier in the design process—weeks earlier than before. That benefit alone gave us a huge boost in productivity. With the pre-defined formal analysis checks, we were able to start up the new environment and run checks right away."

Michele Borgatti, IC Design Manager, UPEK, Inc.

The Customer

Mobile devices can access our most-personal data with relative ease. Security used to be something for government agencies or large businesses, but the digital revolution has brought the issue to everyone's doorstep. That's where California-based UPEK, Inc. comes in. A pioneer in biometric fingerprint technology since 1996, UPEK's goal is to make security simple, whether the solution is for a large federal agency or a personal computer.

The Challenge

At UPEK, one design team handles both the design and verification elements of the flow. For this reason, the designs have to be flexible enough to plug into multiple interfaces in very different computing systems.

"This translates into complex testbenches that activate different use cases and becomes significantly more time-consuming," says Michele Borgatti, IC Design Manager at UPEK. "We needed to find a technique that would allow us to address verification more effectively while also improving time to market for us and for our customers."

The Solution

The UPEK team decided to incorporate an assertion-based verification methodology into its existing design and verification flow.

"Some members of our team had used this methodology in the past and recommended that we adopt Cadence® Incisive® Formal Verifier," Borgatti says. "We were already using Incisive Design Team Simulator in our flow. Our hope was that by adopting an

Business Challenge

- Provide customers with faster time to market

Design Challenges

- Speed the design cycle
- Incorporate an assertion-based verification methodology (across formal analysis and simulation) into an existing design and verification flow

Cadence Solutions

- Incisive Formal Verifier
- Engineering Services

Results

- Sped design cycle by addressing key verification issues upfront in the design
- Increased efficiency and quality of existing flow

assertion-based verification methodology across formal analysis and simulation, we would ease our learning curve and more readily be in a position to take advantage of integration benefits in the Incisive platform and the complementary nature of these technologies. That was indeed the case from the onset."

UPEK Design Team Sees Immediate Results Using Incisive Formal Verifier

One of UPEK's requirements was the ability to address verification issues up front in the design flow.

"By bringing Incisive Formal Verifier into the process, we can now think about verification earlier in the design flow—weeks earlier than before," Borgatti says. "That benefit alone gave us a huge boost in productivity."

> *"We were able to extend the debug capabilities that we had with simulation, and eliminated bugs earlier in the design flow, with the addition of Cadence formal analysis."*

The team was able to come up to speed very quickly using the new assertion-based verification methodology, largely due to automation features.

"We found the pre-defined automatic formal analysis checks in Incisive Formal Verifier to be very useful," Borgatti continues. "We were able to essentially start up the new environment and run checks right away. The complementary nature of simulation coverage points also proved quite helpful."

Assertion-Based Verification Methodology Boosts Confidence at System Level

The UPEK design team was able to quickly achieve overall design quality goals using the new verification environment, which allowed them to work more confidently.

"The first design we created using the new methodology had three modules with many interfaces, and we needed to be certain that we were verifying the interfaces correctly," Borgatti says. "We used Incisive Formal Verifier on two of the modules with a high degree of success."

The combination of Incisive Formal Verifier and Incisive Design Team Simulator provides a complementary set of technologies with strengths at different points of the design and verification flow—formal analysis being ideal early on and for complex-control logic, and simulation being applied for chip-level, end-to-end validation. In addition, unified parsers, common language support, and an integrated debug environment ensure ease-of-use.

"We were able to extend the debug capabilities that we had with simulation, and eliminated bugs in both modules earlier in the design flow with the addition of formal analysis," Borgatti continues. "We were pleased to get such positive results on our first design. The fact that we already knew the environment from our experience with Incisive Design Team Simulator all but eliminated our ramp-up time for getting into the Incisive Formal Verifier technology and debug."

Summary and Future Plans

The UPEK design team experienced early success by adding formal verification to its design process, saving time and improving quality on the first design.

"Based on how quickly we were able to see results using this assertion-based verification methodology across formal and simulation, we're looking forward to what we can achieve as we grow our expertise with the flow," Borgatti concludes.

cadence®

Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com

© 2012 Cadence Design Systems, Inc. All rights reserved. Cadence, the Cadence logo, and Incisive are registered trademarks of Cadence Design Systems, Inc. All others are properties of their respective holders. 7276 02/12 MK/IW/PDF