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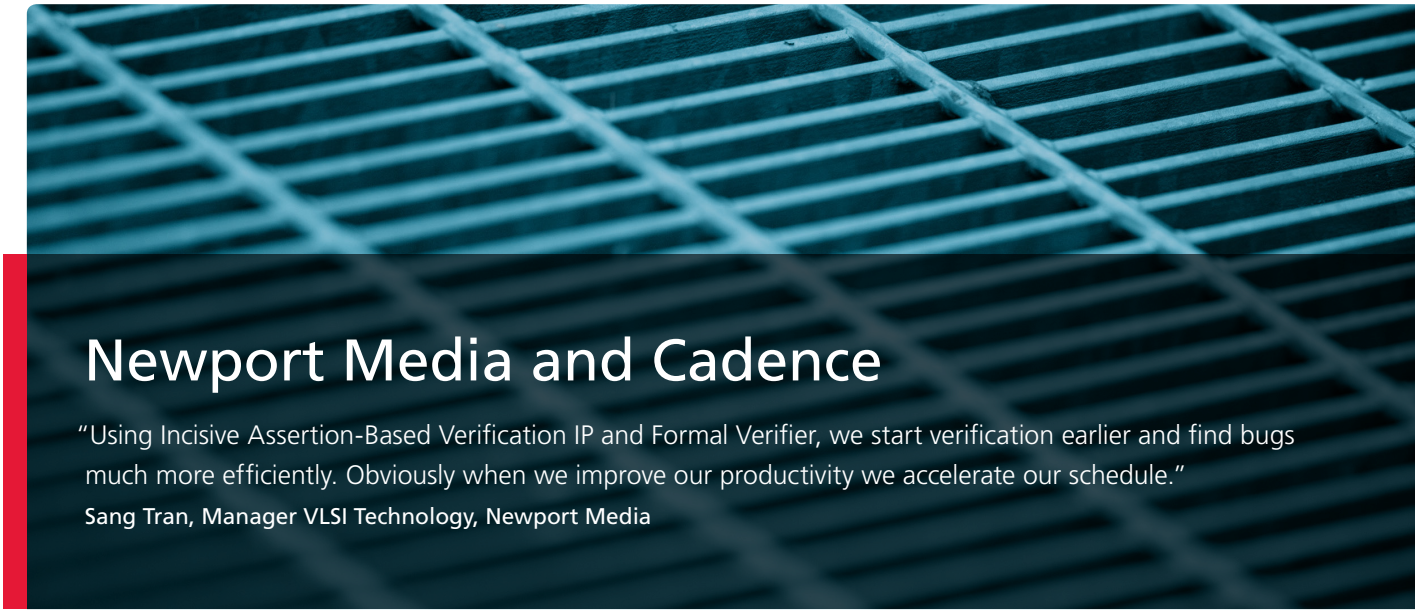

Newport Media and Cadence

"Using Incisive Assertion-Based Verification IP and Formal Verifier, we start verification earlier and find bugs much more efficiently. Obviously when we improve our productivity we accelerate our schedule."

Sang Tran, Manager VLSI Technology, Newport Media

The Customer

Southern California's Newport Media was founded in 2005 with the goal of delivering highly integrated receiver solutions for emerging digital audio and mobile TV applications. A fabless semiconductor company, Newport Media's development team focuses on developing broadcast multimedia architectures and integrated circuit (IC) implementations with unprecedented performance, power consumption, size, and cost-efficiency.

The company's premier product line, Sundance Series, is a multi-standard platform developed to support a wide variety of emerging mobile television standards, including DVB-H, DMB, ISDB-T, and FLO. The single-chip radio-frequency (RF) tuner delivers an advanced user feature set and best-in-class RF noise figure and demodulator Doppler performance.

The Challenge

Newport Media's Sang Tran was tasked with developing the verification environment for a new version of the design featuring an external bus interface. The block under verification featured 40K logic gates, including an AHB master/slave interface, an external microprocessor interface, and a direct memory access (DMA) engine.

"We wanted to address some difficult challenges," Tran says. "In addition to speeding up the verification process, we aimed to write more extensive tests to uncover and explore corner cases."

Business Challenge

- Deliver unprecedented performance, power consumption, size, and cost-efficiency

Design Challenges

- Expose hard-to-find bugs early in the design cycle of AHB master/slave to verify protocol compliance
- Write more extensive tests to uncover and explore corner cases

Cadence Solutions

- Incisive Formal Verifier
- Incisive Assertion-Based Verification IP

Results

- Improved productivity and quality of functional verification earlier in the design and verification process

The Solution

Instant and Insightful Feedback

Though Tran and his team had prior experience with another formal verification tool, they opted to employ the Cadence® Incisive® Formal Verifier solution and Cadence Incisive Assertion-Based Verification IP (VIP).

"I believe each solution has merit, but the Cadence solution really does provide a validated verification approach," Tran says. "I like how the VIP provides instantaneous feedback indicating whether the design complies with the AHB master/slave protocol being tested."

Tran said he had previous experience with verification IP, but found it hard to understand.

"In the past I had to treat it as a black box," he says. "This time I found it to be a much more pleasant experience because I could follow the assertions inside the VIP as if they were in plain English. This solution gives me very clear insight into what each assertion covers."

"I brought up the verification environment in just 15 minutes. I can say confidently that Cadence Verification IP for the AHB protocol saved me several weeks, at a minimum."

Making Quick Work of Verification

The Newport Media verification team took advantage of the Cadence AHB Assertion-Based VIP offering, part of the Cadence extensive Plan-to-Closure VIP portfolio. The AHB VIP, a plug-and-play verification environment that was developed together with ARM, simplifies verification for the ARM® AMBA® AHB™ protocol.

"It's quite amazing," Tran says. "I brought up the verification environment in just 15 minutes."

Incisive VIP provides static analysis and protocol compliance checking. Tran says this Cadence solution provided a serious short cut.

"It's a bit difficult to say exactly how much time it might have taken to create the verification environment myself because that would depend on what kind of test coverage I was aiming to achieve," Tran says. "However, I can say confidently that the Cadence verification component saved me several weeks, at a minimum."

Increased Predictability, Decreased Risk

Newport Media employed Incisive Formal Verifier, together with Incisive Assertion-Based VIP, to enable engineers to begin module verification at the very same time they're being designed. This reduces re-spins and lowers risk.

"I would definitely say we increased our quality and predictability," Tran says. "We saved weeks of engineering time."

Tran said it typically might take weeks to detect hard-to-find corner cases. He stated that Incisive Formal Verifier accurately pinpointed design bugs in about an hour. Because formal analysis does not require the use of test vectors, functional bugs can be detected months before testbench development and simulation can begin.

Summary and Future Plans

Tran said his first experience with Incisive Formal Verifier and Incisive VIP was a valuable one.

"We learned a lot," Tran says. "We can start verification earlier in the process and find bugs much more efficiently. Obviously when we improve our productivity we accelerate our schedule."

Will the Newport Media team be using a similar set of tools for the next verification task?

"Yes, indeed," Tran says. "We're happy with how Incisive Formal Verifier increased our verification productivity. As long as the relevant VIP is available for our next project we'll employ many of the same processes."