Formal Verification based on protocol VIPs

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Track 5 Logic Design
Session 5.5

2-min intro

- Name : Jeroen Vliegen
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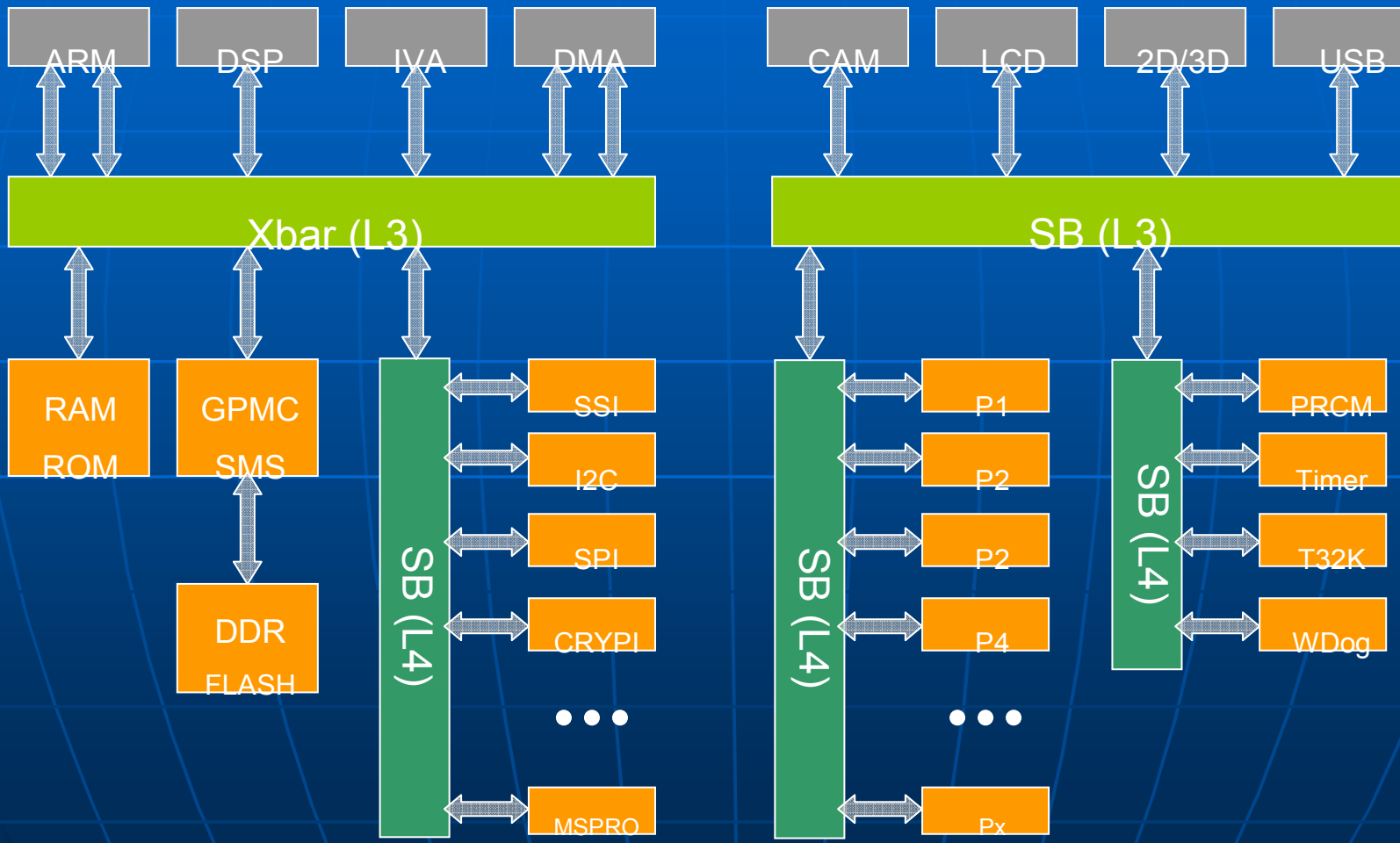
- Lead of TIF Formal Verification group
- 4+1 full-time expert FV engineers
- FV of OMAP / Modem IPs

Outline

- FV using *off-the-shelf* protocol VIPs
  - OMAP / Modem architecture
  - Cadence OCP VIP
    - key concepts
    - verification flow
    - results
- FV using *in-house* developed VIPs
- VIPs as a basis for black box FV
- Conclusions

FV using *off-the-shelf* protocol VIPs

OMAP / Modem architecture (1)



OMAP / Modem architecture (2)

SoC Back-Bone == OCP protocol based

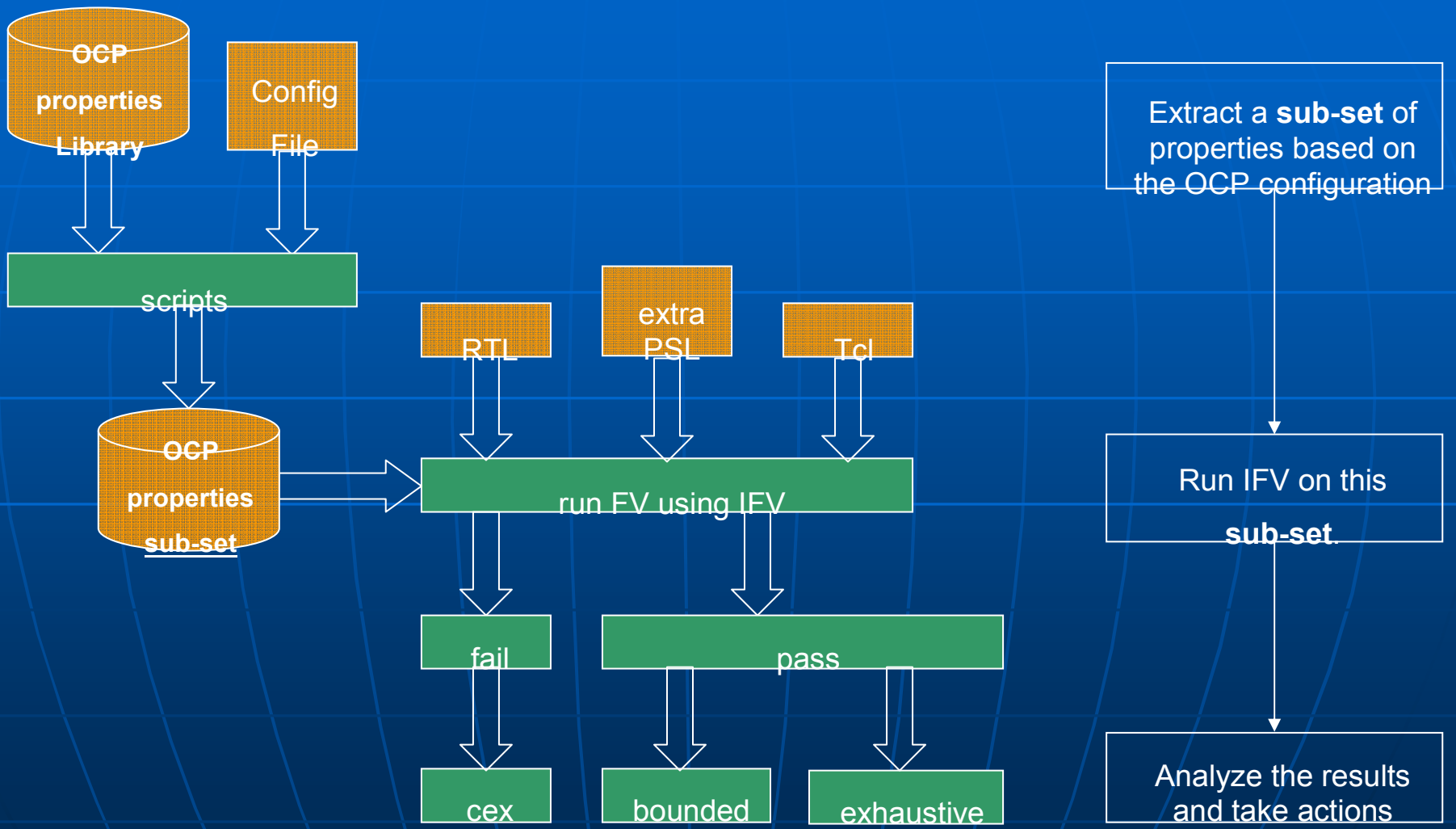
We need an 'easy' way to check that all OCP interfaces are clean (compliant)

Answer : FV using an OCP VIP

Cadence OCP VIP : key concepts

- VIP
  - Verification IP
  - = Pre-coded properties library
  - Languages : PSL + Verilog
- OCP VIP
  - OCP 2.0 properties library
  - Aligned with OCP-IP FVWG compliance plan
  - Targets : OCP interface compliance using FV

Cadence OCP VIP : verification flow (1)



Cadence OCP VIP : verification flow (2)

- fail => cex (counter example)
  - IFV shows the shortest trace which violates the OCP property
  - Debug & fix the RTL
  - Add missing constraints, exclude false violations
- pass => bounded
  - Up to a certain depth of the state-space, IFV could not violate the property
  - Apply a higher effort, switch engine, reduce the circuit size (generics), add abstractions, …
- pass => exhaustive
  - The property could never be violated
  - We're done !!

Cadence OCP VIP : results (1)

- Run time – some numbers
  - A typical slave IP (~1K FFs) is proven OCP compliant (or not!) within ~30 minutes
  - Most of this time is spent on setting up the environment (automate as much as possible)
  - The actual IFV proof-time ~1 to 5 minutes
  - Larger IPs (~10K FFs) or more complex circuits (OCP masters) require a bit more effort (~hours)
  - If the circuit is too large (sub-system), the user must isolate the OCP circuitry (eg. bridges) and only prove those
  - Hence good partioning is a key to succes

Cadence OCP VIP : results (2)

- TI flow
  - The OCP VIP is part of our flow
  - OCP formal proof == IP acceptance criterium
  - An average OMAP/Modem contains ~50 IPs
    - The majority are simple slaves => good
    - The rest are huge master sub-systems => more tricky
- Bugs
  - Several bugs were found on pre-verified IPs (C & E)
  - Most bugs found are hard-to-find corner cases
- Pass quality
  - Most properties have an exhaustive pass !!

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Power Management VIP

- VIPs maximize the verification ROI & overall TTM
- Each IP in our SoCs has
  - 1 or more OCP interfaces (master / slave)
  - 1 or more TI proprietary Power Management interfaces
- Hence the need for a
  - a Power Management VIP
  - developed in-house

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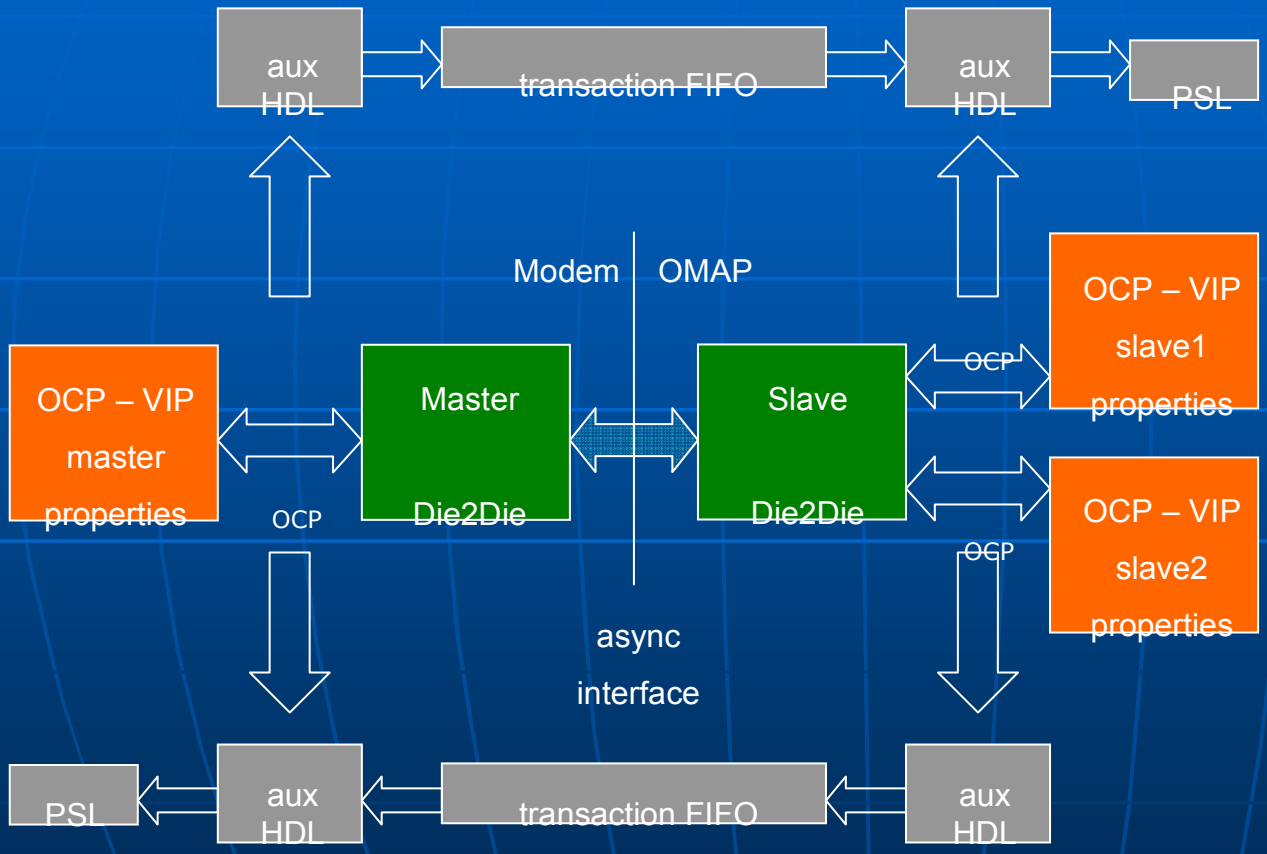
Main reasoning

- First
  - formally prove OCP compliance
  - formally prove the Power Management protocol
- Second
  - re-use the OCP / Power Management *constraints*
  - extract high-level black box functional properties
  - prove them
- Case study : die-2-die interface

Case Study : die-2-die interface



Prove OCP compliance

Add high-level bbox properties and verify them

Examples:

1) transaction transformations (burst4 to burst8)
2) transaction ordering
3) secure reset

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Conclusions

- VIPs enable a fast and exhaustive interface verification of parallel protocols (OCP, PM)
- VIPs provide (verified) constraints to enable higher-level black box properties development
- VIPs can be bought over-the-shelf, therefore reducing the development effort to 0
- Proprietary protocol VIPs can easily be developed in-house
- Overall : VIPs increase ROI & decrease TTM

! Thank you !

Q & A