cadence®

Enterprise System-Level (ESL) Verification Solution—Beyond "First Silicon Success"

Today's complex integrated-circuit (IC)-based embedded systems, characterized by increasingly sophisticated hardware and software, require more than conventional verification methods. Successful, predictable verification requires automated test generation, increased visibility across all phases of verification, and reliable methods for isolating bugs across hardware and software domains. Using Cadence® Incisive® Enterprise System-Level (ESL) Verification Solution, electronics systems manufacturers can achieve fully predictable system-level quality and reduce time to market by 50 percent.

Contents

Introduction.....1

Enterprise System Level (ESL) Verification 2

Cadence Incisive ESL Verification Solution.....2

Toward Enterprise System-Level Verification 4

Introduction

Today, more than 70 percent of integrated circuit (IC) design starts are system-on-chip (SoC) ICs comprising embedded processors and software. In this environment, traditional objectives of achieving first silicon success remain important, but are no longer the sole determinant of success in new product development. Increasingly, systems manufacturers realize that product success depends on the full functionality of the entire system—including embedded software, system-level bus protocols, and the interaction between these within the hardware design.

For engineers, however, system-level verification capabilities have not kept up with increasing complexity in hardware and software components and their interfaces. To achieve predictable closure at the system level, electronics companies need verification capabilities that better orchestrate the efforts of multiple engineering specialists involved in the development of next-generation products that combine more complex hardware with more sophisticated software.

The Cadence® Incisive® Enterprise System-Level (ESL) Verification Solution provides a unified approach to system verification through automated test generation, system-wide management, and high-performance engines. With this new approach, multiple engineering specialists can for the first time tackle cross-domain verification and debug needed to achieve success in more complex system-level products—in less time.

For engineers, increased product complexity means a rapid increase in the number of tests created to verify a growing feature list and validate more complex usage scenarios. Yet, engineers must cope with the reality that each test performed at the chip or system level can require more than a week of run time. Worse still, tests performed at the block level typically cannot be leveraged at the chip level—much less at the system level—requiring signif-icant effort to recreate suitable testbenches as designs move from block- to chip- to system-level verification phases.

As both hardware and software engineering teams continue to verify, debug, and refine their designs in parallel, few organizations are equipped to coordinate bug resolution and design refinement across system-level hardware/software interfaces. Teams will inevitably uncover many bugs on a continuous basis, forcing each team to freeze development while waiting for the other team's response—or risk a rapid divergence between hardware and software components.

Instead, detailed upfront planning can help teams uncover problems well before implementation, simply because team members communicate more effectively during the verification planning phase of the project. Furthermore, effective management of the bug reporting and resolution process can address the high volume of bugs and ensure each team immediately becomes aware of potential hardware/software conflicts.

Enterprise System-Level (ESL) Verification

The solution for addressing emerging system-level verification requirements lies in leveraging successful application of metric-driven planning methods and sophisticated verification technologies to encompass both hardware and software. Today, verification engineers are passing along advanced techniques for block-level verification to those concerned with the overall system-level quality. Indeed, verification engineers can quickly find corner-cases thanks to recent advancements such as improved metric-driven planning techniques and much improved automated testbench, simulation, acceleration, and emulation engines. Similarly, engineers can exploit advanced verification technologies such as debugging capabilities within simulation and SystemC® models, more coverage-driven and metric-driven capabilities earlier in the process, and the ability to manage enterprise system-level verification from initial plan to full system-level closure.

Enterprise system-level (ESL) solutions formalize this cross-fertilization of verification methods, combining RTL and higher level abstraction by leveraging proven concepts in RTL block-level verification and applying these to system-level verification. This new approach provides unified system verification, addressing cross-domain verification of hardware and embedded software, while bringing together design and verification from initial plan to full system-level closure. At the same time, this approach addresses productivity challenges. It combines automation for hardware and embedded software test generation and high-performance engines into a single solution—under the umbrella of a comprehensive verification management capability—that provides visibility into the progress of block, chip, and system verification.

This expanded notion of ESL verification addresses the need for multiple levels of abstraction within a single verification environment, while supporting the individual needs of multiple specialists within the context of the overall verification objective. It combines metrics, automated reporting, and other automation techniques to reduce the effort for team members to communicate continuously about their parallel efforts. At the same time, it normalizes the language of the hardware and software teams to metrics they can each understand. As a result, hardware and software engineers can find bugs earlier, shortening time-sensitive development schedules. By improving engineers' ability to predict system performance and functionality, this new definition of ESL can help ensure first-pass success for both silicon and software.

Cadence Incisive ESL Verification Solution

The comprehensive Cadence Incisive ESL Verification Solution provides system-wide verification management and automated scenario generation, executing on high-performance engines enabled by a comprehensive development ecosystem. This solution helps electronics systems manufacturers ensure total system coverage driven by the Incisive Plan-to-Closure Methodology for unified verification.

This unique methodology combines planning, implementation, and validation within a consistent environment for IC design and system-level co-design. In this approach, the entire process is driven from a central plan, which serves as the launching point when applying this comprehensive methodology. Here, the development team approaches the verification problem from multiple fronts, drawing on documented best practices, executable examples or templates for use by engineers as they deploy the methodology and new technologies. Using this form of methodology, traditional design teams and larger enterprise efforts can achieve greater coverage of more complex blocks, chips, and systems in less time.

The Cadence Incisive ESL Verification solution automates this methodology through its key components:

Incisive enterprise manager

Incisive Enterprise Manager provides system-wide management capabilities that extend proven hardware plan and metric-driven verification management to embedded software and system-level verification. This approach enables design teams to apply the verification plan for embedded software and system-level verification requirements with automated collection of coverage information, and annotation of progress to the plan. For monitoring verification progress and optimizing enterprise resources, the platform provides coverage hole analysis, test ranking, correlation analysis, and charting of metrics with a hierarchical view of hardware, software, and system activities. With these capabilities, system manufacturers can achieve predictable closure and quality assurance with total system coverage aggregated across hardware, software, and system-level verification activities.

Incisive software extensions (ISX)

Incisive Software Extensions apply proven techniques from advanced hardware verification to embedded software and system-level verification. With this capability, engineers for the first time can apply constrained-random and coverage-driven techniques to automate the generation of system scenarios comprising software routines, hardware functions, and system-level interface transactions. For software, Cadence provides a software Universal Verification Component (UVC) methodology and support, which typically results in minutes to hours of development time. The software UVC is a new form of verification IP that provides software sub-routines in various sequences to the automation environment and measures coverage of those function calls. During verification, a generic software adaptor lets software engineers exercise SoC software at varying levels of performance and accuracy on multiple target engines without changing the environment, model, or physical chip. As engineers test their software, integrated Incisive hardware/software debug capabilities provide additional failure analysis features.

Incisive Palladium® III and Xtreme® III for hardware-assisted verification

High-performance Incisive engines offer the highest throughput engines for simulation-based, hardware-assisted, and testbench automation, accessed from the system-wide management and automation environment. Palladium® III provides up to 2Mhz performance and provides a high-speed transaction interface that allows engineers to integrate hardware-assisted verification with the constrained-random ESL verification capabilities of Incisive Software Extensions. Furthermore, engineers can leverage Incisive high-speed automated system-level test generation to automatically generate transaction-level system and embedded software scenarios. During verification, Incisive Enterprise Simulator can link high-speed SystemC transaction-level reference models to the constrained-random ESL verification capabilities (Incisive Software Extensions).

Common SimVision debug environment

The SimVision environment provides a unified cockpit for analyzing results. Furthermore, enhancements to the SimVision environment allow engineers to control third-party embedded software debuggers in parallel with transaction- and signal-level hardware debug, leveraging the failure analysis information from Incisive Enterprise Manager.

Achieving true enterprise system-level verification requires a comprehensive verification ecosystem that combines the platform and software with a broad array of processor models and verification IP needed to support advanced SoC development. Cadence is helping develop a strong ecosystem to provide support around the Incisive ESL Verification Solution; it will support embedded processors and software debuggers, bridging system-level design, integration, and verification requirements across the full enterprise and across the broader ecosystem. Various SoC engineering specialists can debug, automate the generation of system-level and embedded-software random scenarios, and track the coverage metrics of interactions between software and hardware in embedded systems. Furthermore, engineers can model the processor at a high level of abstraction or in hardware, while debugging embedded software running on a workstation, PC, or emulator. Other elements of the Incisive ESL ecosystem give designers access to powerful cross-probing, debug, and analysis between customer hardware design and their embedded software environment for system-level verification with Incisive Palladium III and Incisive Enterprise Simulator.

Toward Enterprise System-Level Verification

As both hardware complexity and software sophistication continue to rise sharply in complex IC-based embedded systems, conventional verification methods are falling further behind in their ability to address mainstream hardware/software development methods. As market pressure squeezes project schedules, predictable verification closure of larger, more complex system designs demands automated test generation, better visibility across all phases of verification, and more reliable methods for isolating bugs that involve both hardware and software domains.

The Cadence Incisive ESL Verification Solution for the first time provides unified co-verification capability with system-wide management, coverage, and analysis including hardware and embedded software. With this solution, multiple engineering specialists work at multiple levels of abstraction within a single verification environment, using a single debug environment for hardware and embedded software. Its ability to automatically generate tests for hardware and embedded software provides the productivity boost needed to ensure quality; verification management capabilities provide the visibility needed to ensure predictability.

Using this solution, electronics systems manufacturers can achieve a 50 percent reduction in time to market with fully predictable system-level quality. By automating hardware/software co-verification prior to silicon availability, engineers can reduce the risk of failures arising from subtle errors within hardware/software interactions. At the same time, the ability to perform hardware-assisted verification runs at multiple levels of abstraction delivers improved verification throughput. For engineers, the Cadence Incisive ESL Verification Solution enables a single, unified methodology and integrated debug environment to address the growing challenges of hardware/software co-verification. For electronics systems manufacturing companies, this solution reduces the risks and uncertainties associated with complex embedded systems to deliver higher quality products in less time.