SUCCESS STORY

CADENCE AND UNISYS

Design with Verification Flow Starting with Incisive Formal Verifier Boosts Productivity and ASIC Quality at Unisys.

Unisys is a worldwide technology services and solutions company. Unisys consultants apply expertise in consulting, systems integration, outsourcing, infrastructure, and server technology to help clients achieve secure business operations.

Inspired by mainframe designs, the Unisys ES7000 products deliver enterprise levels of performance, availability, and flexibility. Unisys ES7000 servers are the foundation for a variety of solutions, including those supporting large databases and large numbers of users with high I/O throughput and enterprise-capable scalability, performance, and resilience. In an effort to increase productivity and accelerate their time to market, the Unisys design team employed the Cadence Incisive® Formal Verifier along with Incisive Design Team Simulator and Incisive Palladium® accelerator/emulator.

CORPORATE PROFILE

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DESIGN CHALLENGE

- Expose hard-to-find bugs early in the design cycle of the complex ES7000 Real-Time Capacity Server Series
- Verify design blocks prior to testbench simulation for faster time-to-market

CADENCE SOLUTION

- The Cadence Incisive Formal Verifier technology as part an assertion-based verification flow was incorporated into the production design flow complementing Incisive Design Team Simulation and Incisive Palladium Emulation
- Design with Verification in mind started with logic design teams early in the project cycle minimizing lengthy tail-end functional iterations
- Productivity and product quality were dramatically increased

CADENCE PRODUCTS AND SERVICES

- Cadence Incisive Formal Verifier, Incisive Design Team Simulator, and Incisive Palladium Emulator

DELIVERING A CAPACITY-ON-DEMAND SERVER SOLUTION

IT organizations rely on Unisys ES7000 Real-Time Enterprise (RTE) servers to meet their availability, manageability and performance requirements.

What's more, the servers deliver immense "capacity-on-demand" benefits to businesses and government agencies that anticipate growing processing requirements or seasonal workload spikes. The design of the Unisys ES7000 Real-Time Enterprise server series includes complex server ASICs that interface with processors, system memory, and I/O channels.

RESPONDING TO VERIFICATION BOTTLENECKS

The verification team at Unisys had experienced costly delays in block-level verification on past ASIC designs. Given the increasing complexity of designs

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Steve Guarierri, Vice President, Platform Development, Unisys

before them and growing quality concerns, they decided to find a solution capable of overcoming verification bottlenecks.

"We tried various metric-driven simulation approaches that really were not helping us enough," said Steve Guarierri, Vice President of platform development at Unisys. "The iteration cycles for verifying the block level components of the ASICs were problematic," he continued. "Cycles were taking too long and starting too late in the design process to significantly improve our early verification process."

In response to the pressing problem, the group chose to add formal analysis for interactive block-level testing starting at the desktops of logic designers, selecting the Cadence Incisive Formal Verifier (IFV). Incorporated into the Unisys design flow, IFV would help the team reap the benefits of assertion-based verification via formal, simulation, and emulation.

ACCELERATING BLOCK DEVELOPMENT AND INTEGRATION

Guarierri reported that the IFV platform delivered a far faster and more efficient methodology. "By using it early in the design cycle our overall bug find and fix rates have gone up. The logic design team has been able to quickly isolate the problems and instantly iterate before even thinking about the testbench development and simulation verification to come months later," he explained. "We definitely have a time-to-market acceleration solution here."

IFV allows Unisys to start verification months earlier, while designers create the RTL and verify its correctness with white-box assertions. Black-box interface assertions are also used and serve as a contract between the blocks, and are also leveraged to significantly help in dynamic simulation via Incisive Design Team Simulation by hardening the interfaces, then used again at the system level in Incisive Palladium emulation to accelerate debug. Overall, the logic design and verification engineering teams can quickly converge on correct block implementation and speed up the chip integration time.

Complex functional problems are exposed much earlier, which helps with overall verification closure and increases the odds that first silicon is successful.

"On one project, Incisive Formal Verifier exposed a significant number of functional problems very early in the project cycle within a three-month period," said Ross Weber, Senior Design Engineer at Unisys. "Without it, I would have spent months developing specific tests and simulations, finding these bugs much later, and most likely spending lengthy iteration cycles for most of these. Moreover, a few of the design problems caught with formal analysis could potentially have been missed by simulation and emulation due to their complex nature. Hence, IFV minimized the chance of costly design iterations late in the design process and possible project delays."

A MORE PRODUCTIVE APPROACH FOR VERIFYING COMPLEX LOGIC

The Unisys team experienced great productivity gains in verifying complex logic for buffer control, arbitration, maintenance controller functions, state machines, interrupt controller, and more.

"We learned that throwing more simulation vectors and emulation cycles at the complex verification problem was not enough to affect productivity," said Guarierri. "But leveraging formal verification and the assertion-based verification flow by both logic design teams and verification teams does improve producivity. It allows us to quickly test functional corner-case scenarios during the early block bring-up phase, which may not even come up as part of the initial test plan."

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