INVENTIVE

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Low Power Design of the DLX Processor Using the Encounter Platform Session #: 4.13

Madhuparna Datta, Cadence Design Systems
Shalini Sharma, Freescale Semiconductor Inc
Harjot Singh, Cadence Design Systems

Agenda

- **Low Power Design of DLX Processor Core**
  - Overview of DLX Processor Core
  - RTL Level Power Estimation Methodology
  - Application of standard Low Power Design Techniques
  - Redesign of Critical Portions of Design to reduce Power
  - Front End and Back End flow
  - Conclusions

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Overview of DLX processor core

- DLX is a generic 32 bit RISC microprocessor
- Used for academic Purposes
- 32 thirty two bit registers
- 5 stage Pipeline
- Why was DLX chosen?
  - Based on observations about most frequently used primitives in programs
  - Good architectural model for study
    - Popularity
    - Easy to understand

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Overview of DLX Processor Core

- **INSTRUCTION SET**
  - Fixed 32 bit instruction set for improved code efficiency.
  - Register , Immediate and Jump type instructions
  - Access to objects other than byte must be aligned.
  - Load / Store architecture
  - Conditional Execution
  - Instruction Execution, maximum 1 instruction per cycle

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Overview of DLX Processor Core

- **MEMORY INTERFACE**
  - 32 bit data interface to Instruction cache for accessing fixed 32 bit instructions
  - 32 bit address bus to Instruction cache
  - 32 bit data interface to Data cache
  - Signals to indicate nature of access byte/word/double word
  - Signals to indicate type of access read/write to Data cache

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Overview of DLX Processor Core

- **INTERRUPTS**
  - External interrupt to halt program execution.
  - Interrupt to stall the pipeline.
  - Signal to clear the Interrupt.
- **STATUS SIGNALS**
  - Signal to indicate status of pipeline empty or not empty

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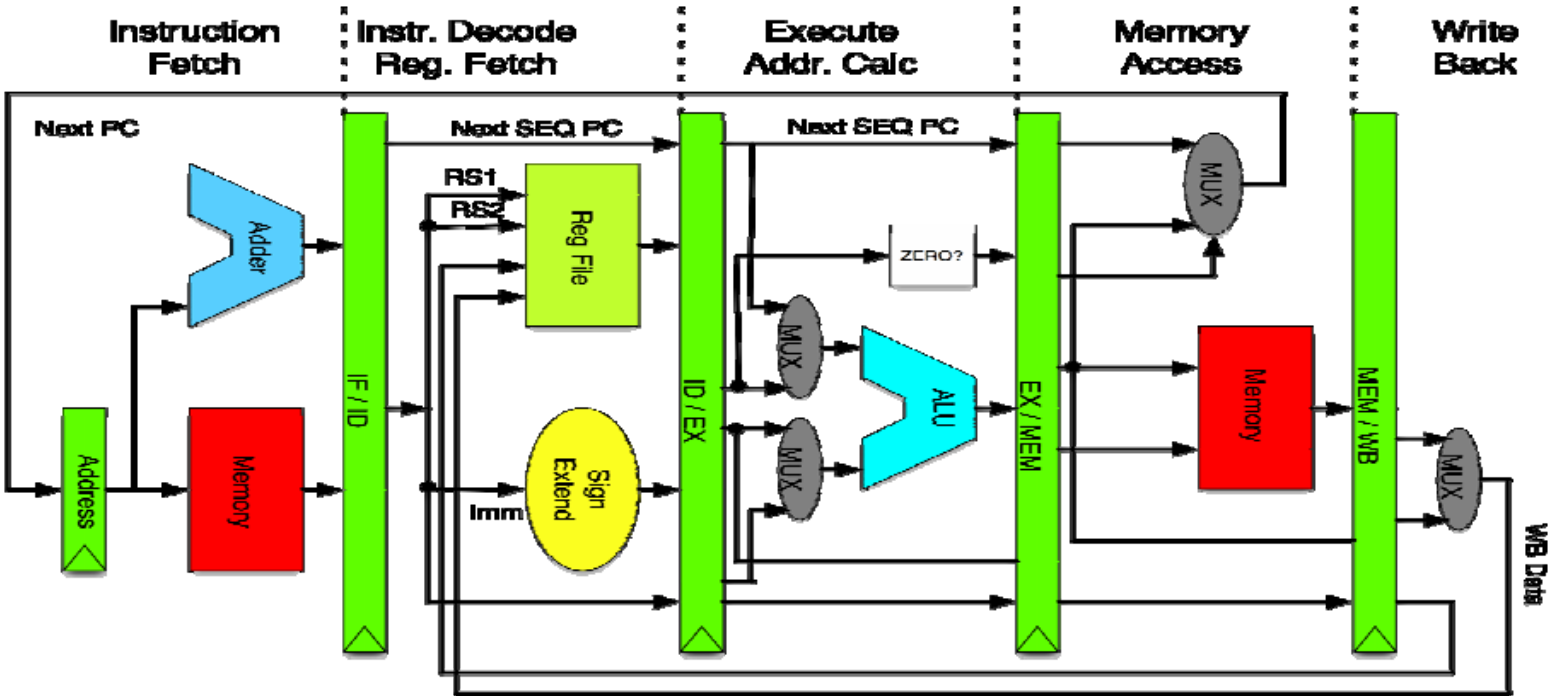
5 Stage Pipeline of DLX



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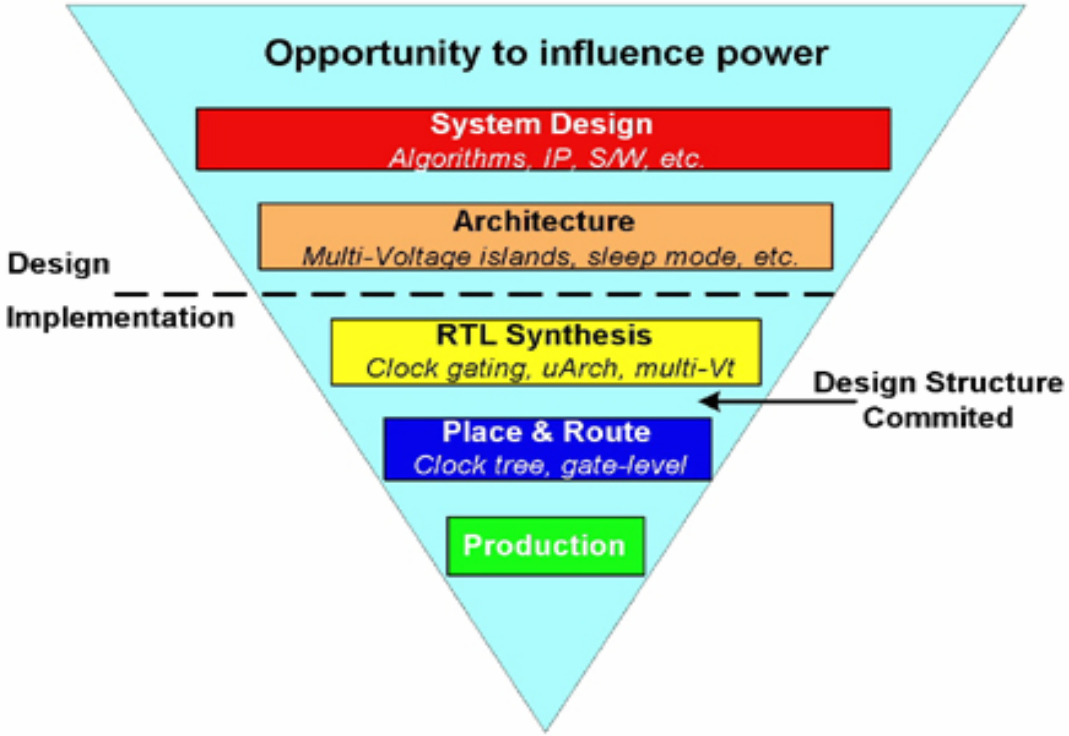
Why Optimize at RTL?

- Power Savings are maximum at RTL level



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RTL Level Power Estimation

- Accuracy of RTL level Power Estimation
  - Functional Vectors used For Power Estimation
  - Libraries/PVT conditions used for Power Estimation
  - Interconnect Model / Wire-load Model used for Power Estimation.
  - Level Of Hierarchy where Power is analyzed
  - Power Calculation

- Power Estimation Results of DLX Processor Core

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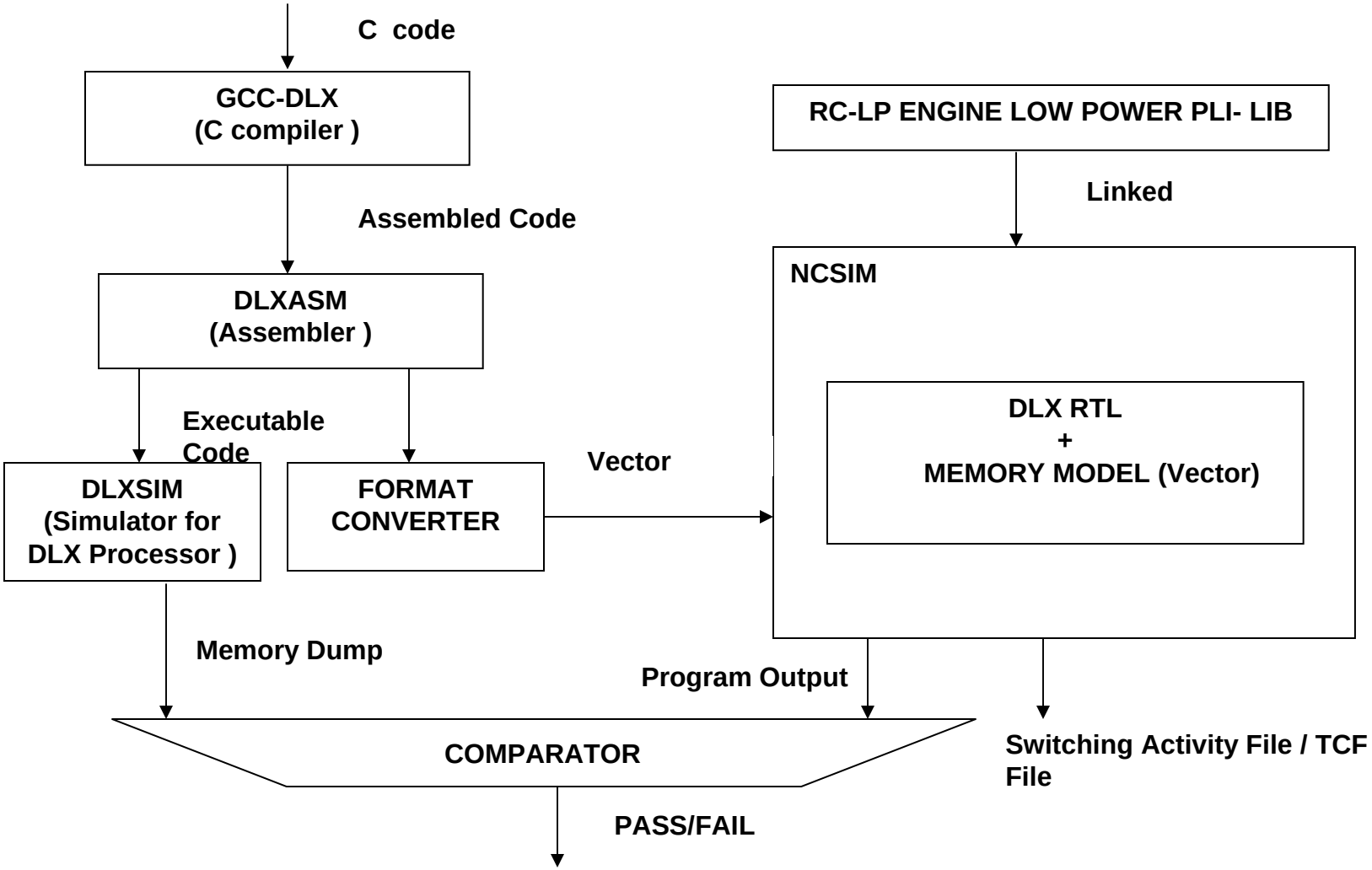
Vector Generation Flow for DLX Processor Core



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Libraries/PVT/Interconnect Model used for Power estimation

Libraries/PVT	Best Case/P_{best} V_{max} T_{min}
Interconnect Model	1st set with Enclosed wireload 2nd set with PLE
Level Of Hierarchy	Each Stage of pipeline of 5 Stage pipeline of DLX

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Power Calculation in RC-LP Engine

$$P_{total} = \sum P_{instance} + \sum P_{net}$$

$$P_{instance} = \sum P_{internal} + \sum P_{leakage}$$

$$P_{net} = \frac{1}{2} C \times V^2 \times f \times TR$$

$$P_{internal} = \sum_{per\ arc} TR_{arc_{ij}} \times \phi(SR_i, C_j) + \sum_{per\ pin} TR_i \times \phi(SR_i)$$

$$P_{leakage} = \sum_{state=1}^{k} P_{state_leakage} \times probability_{state}$$

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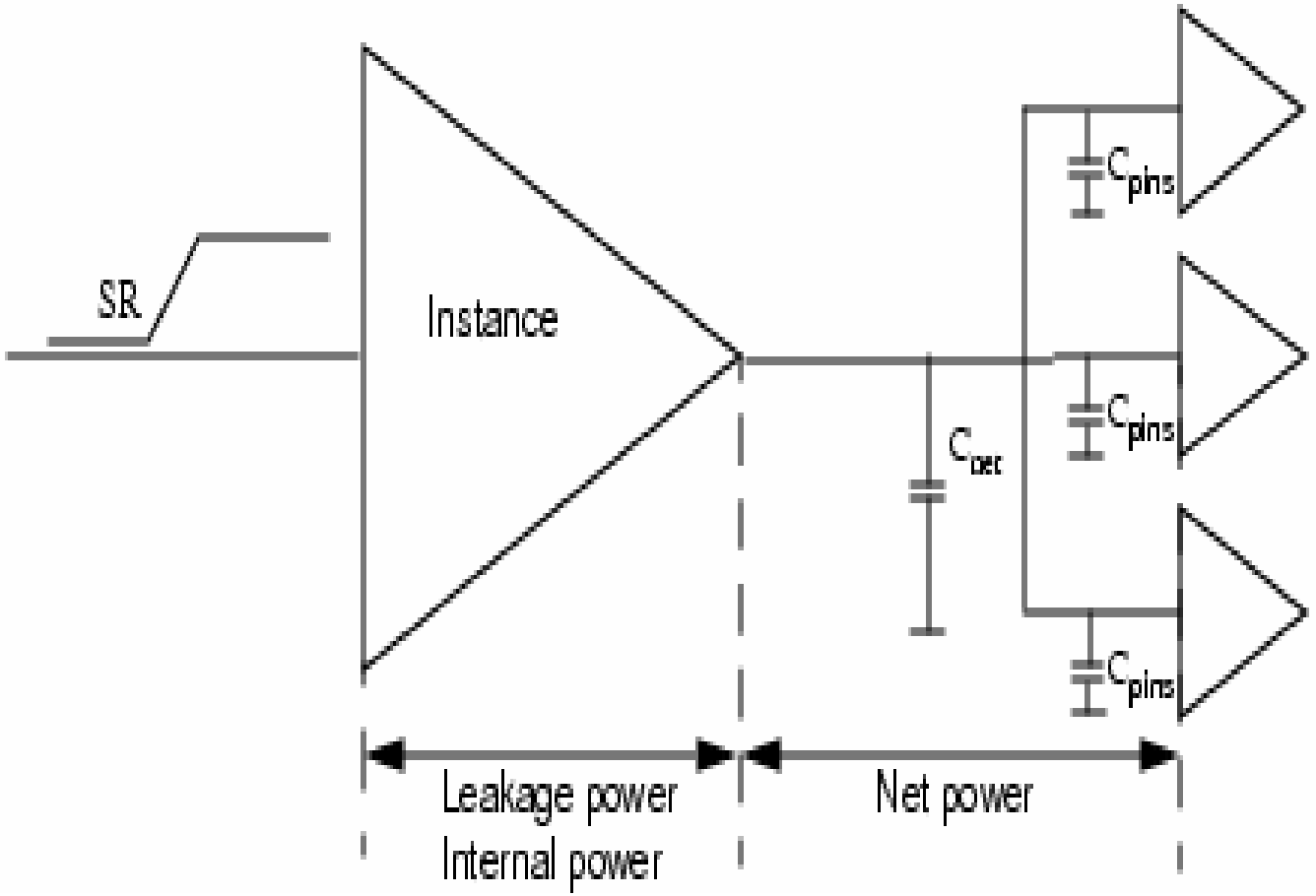
Power Dissipation Model



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Power Estimation of DLX Processor Core

- DLX Process was Benchmarked for power using set of 4 test cases written in C
  - MATRIX MULTIPLICATION
  - FACTORIAL
  - FIBONACCI
  - ATOI
- Frequency of operation chosen is 100 Mhz

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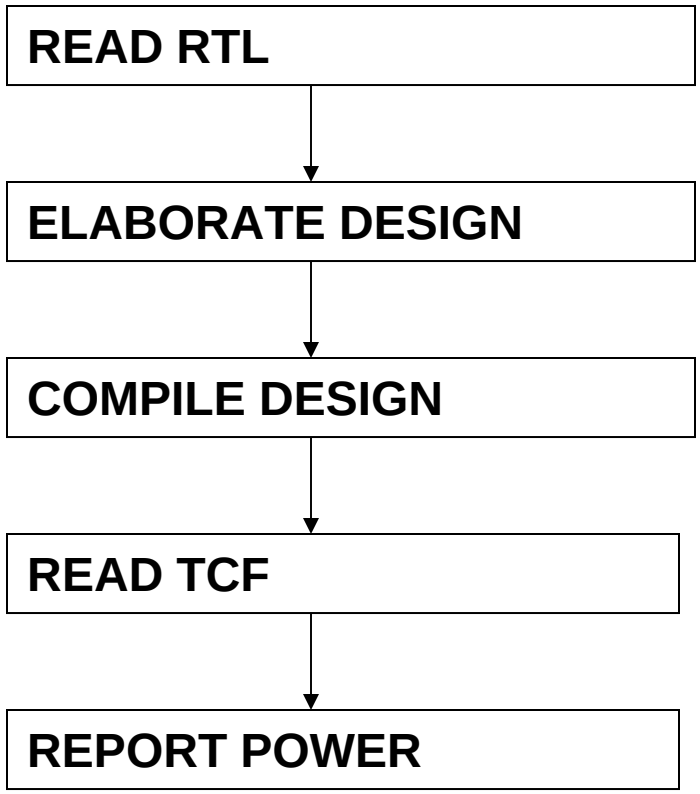
Power Estimation Flow



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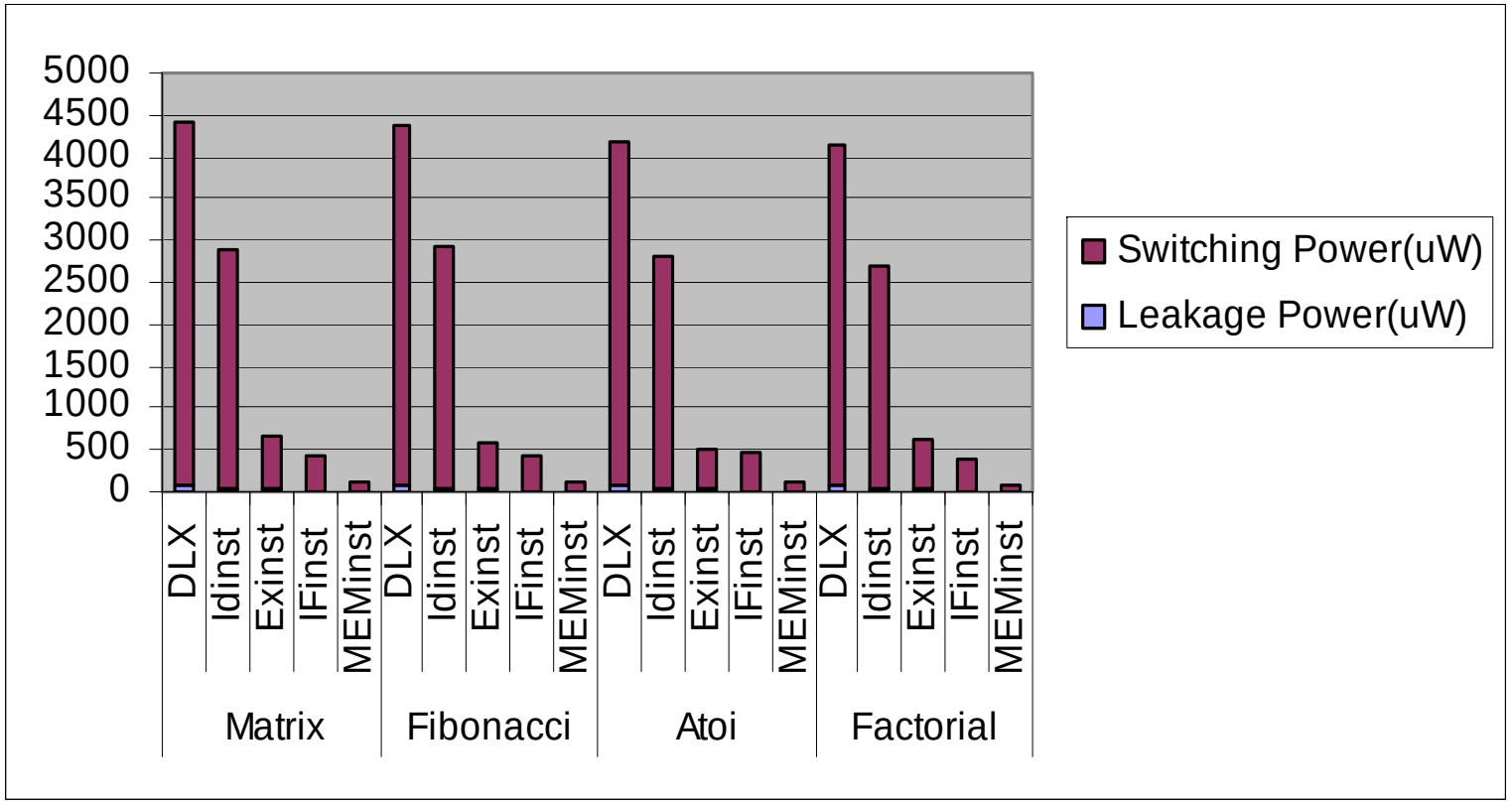
Power Estimation Results of DLX Processor Core

Wireload model

Max Power: 4.42mW (matrix)



60% power consumed in IDinst. Only 2% of total is leakage!!

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Power Estimation Conclusion of DLX Processor Core

Wireload model

- Power Cosumption of DLX processor core is 4.4 mW using worst functional vector with switching power =4.3 mW and leakage power =86.29 uW.
- About 61 % of Total dynamic power is consumed in ID unit of DLX Processor Core
- To achieve any Reduction in power, ID unit should be targeted

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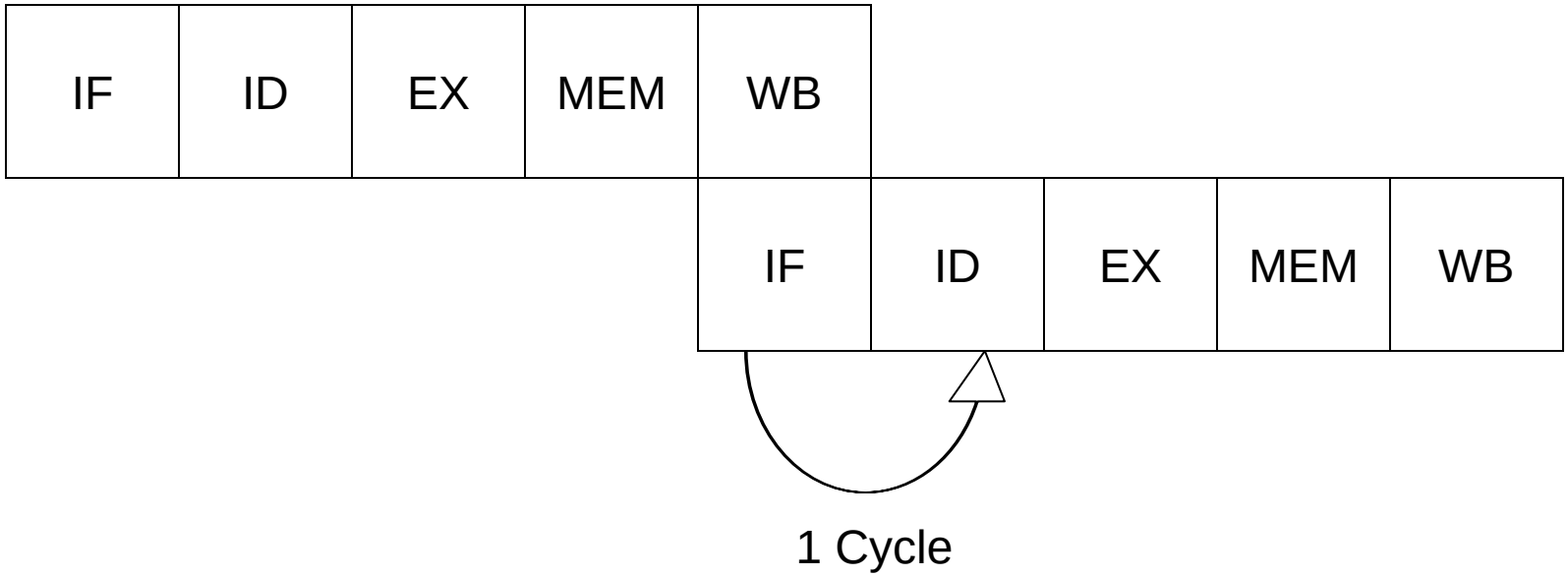
Revisiting DLX PIPELINE



Scheduling For Read After Write to a Register in Pipeline

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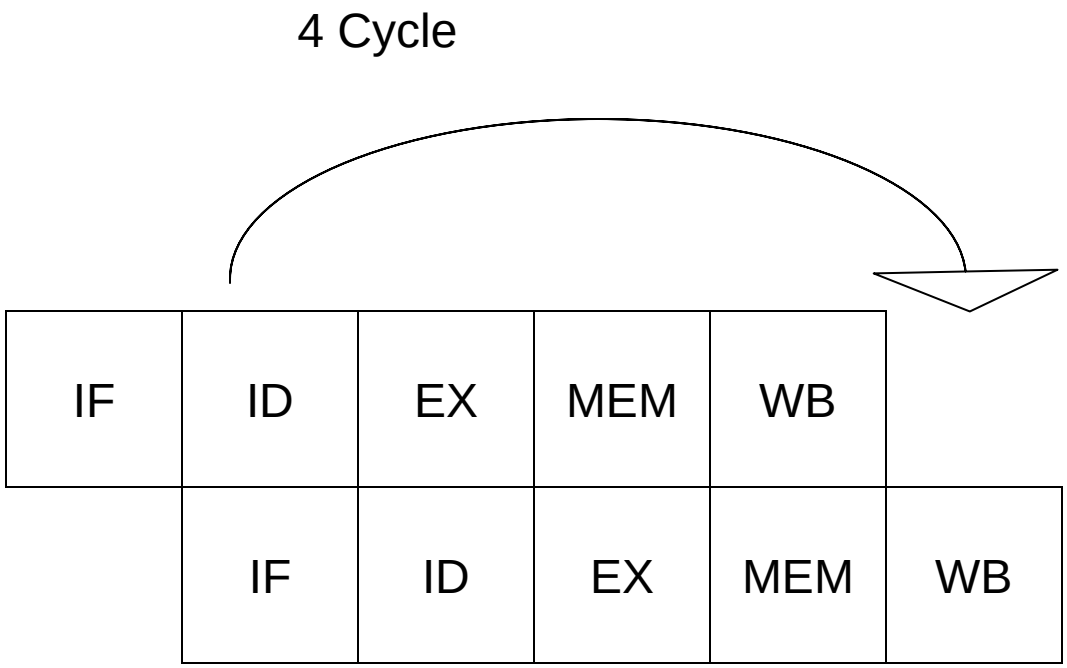
Revisiting DLX PIPELINE



Scheduling For Write After Read to a Register in Pipeline

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Design Optimization for Power

- Register File read occurs in ID stage and Write in WB stage
- 4 cycle delay exists for Write after Read operation to the same register in the register File
- 1 cycle delay exists for Read After Write from a register in the register File
- DLX Register File used pos edge Flip Flops
- Timing Relationship for read after write and write after read to a particular register allows us to replace all registers with negative level sensitive latches with no change in functionality .

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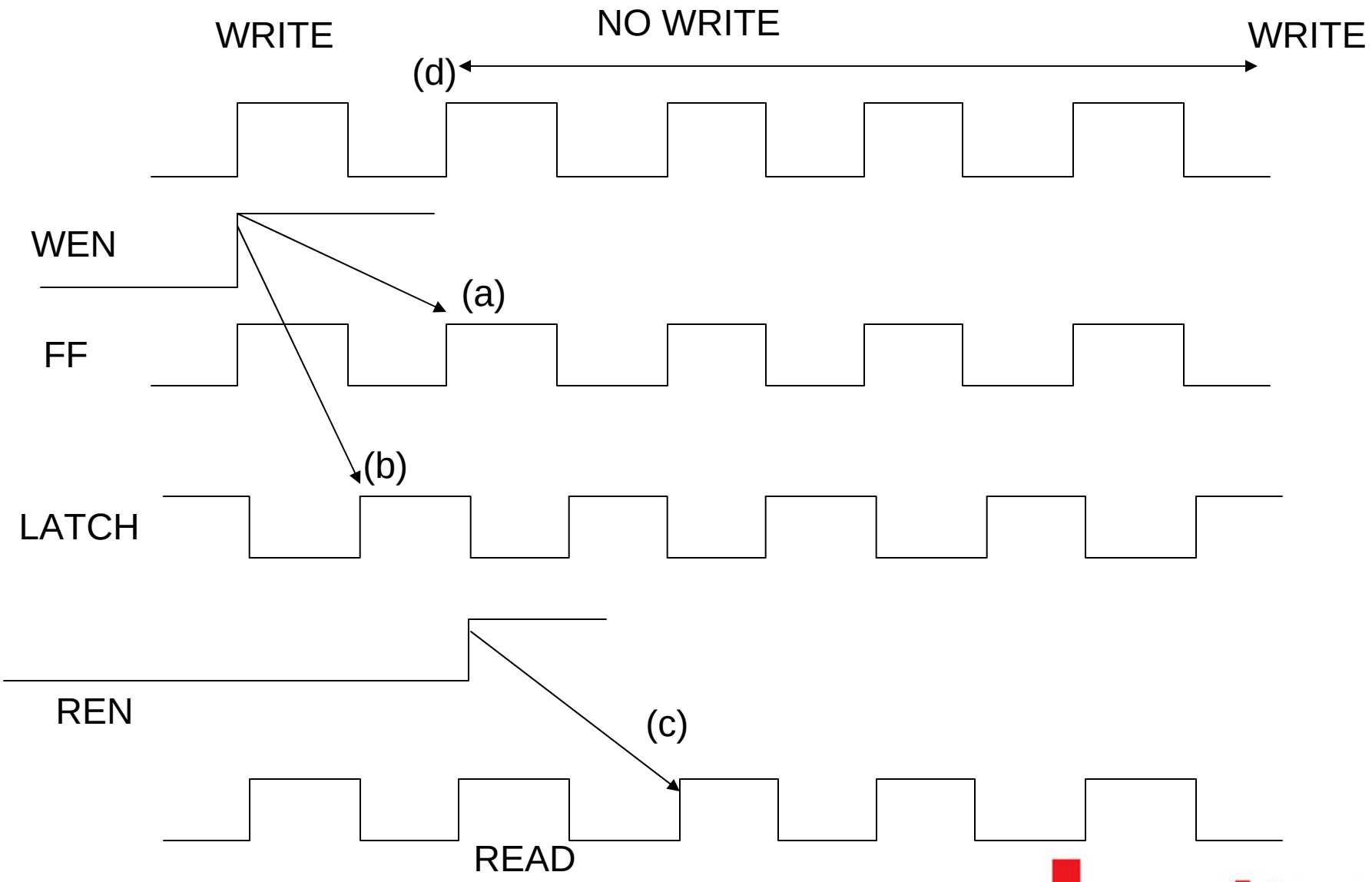
Timing Diagram



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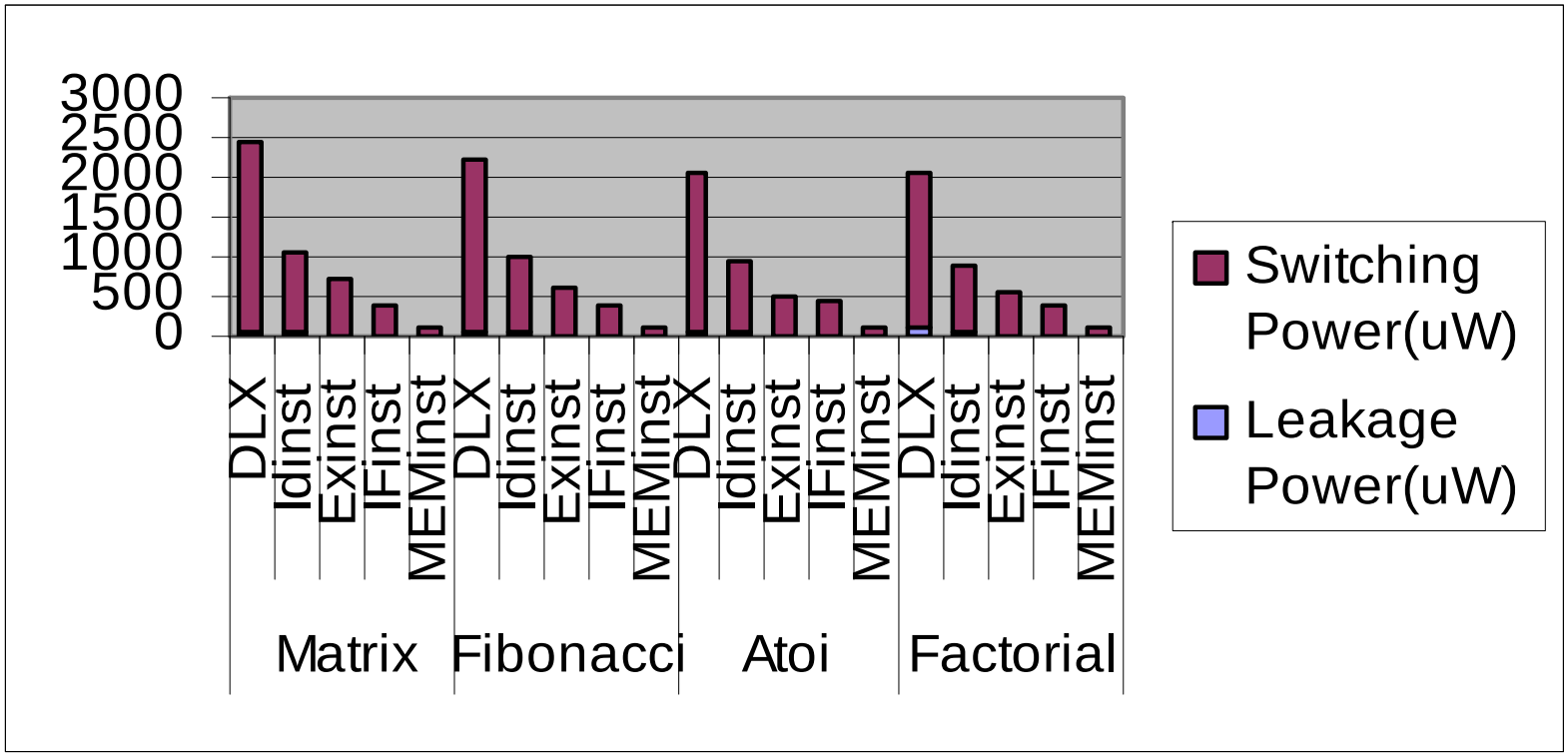
Power Estimation of DLX Processor Core

Wireload model



Baseline of NewregFile reduces power by 45%

Max Power is 2.41 mW (matrix)

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Low Power Implementation of DLX Processor Core

- Synthesis Methodology
  - Clock Gating
  - Operand Isolation
  - Leakage Power Optimization
  - MSMV Methodology
  - Power Constraints

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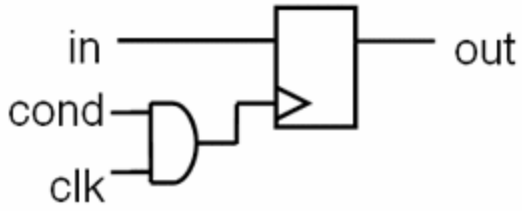
Clock Gating

- Clock gating is stopping the clock during the idle period when the register is shut off by the gating function.



- Power is saved in the gated-clock circuitry.
- For inserting CG in RC
  - set_attribute lp_insert_clock_gating true
- To merge clock-gating instances, we used the following command
  - clock_gating declone [-hierarchical]

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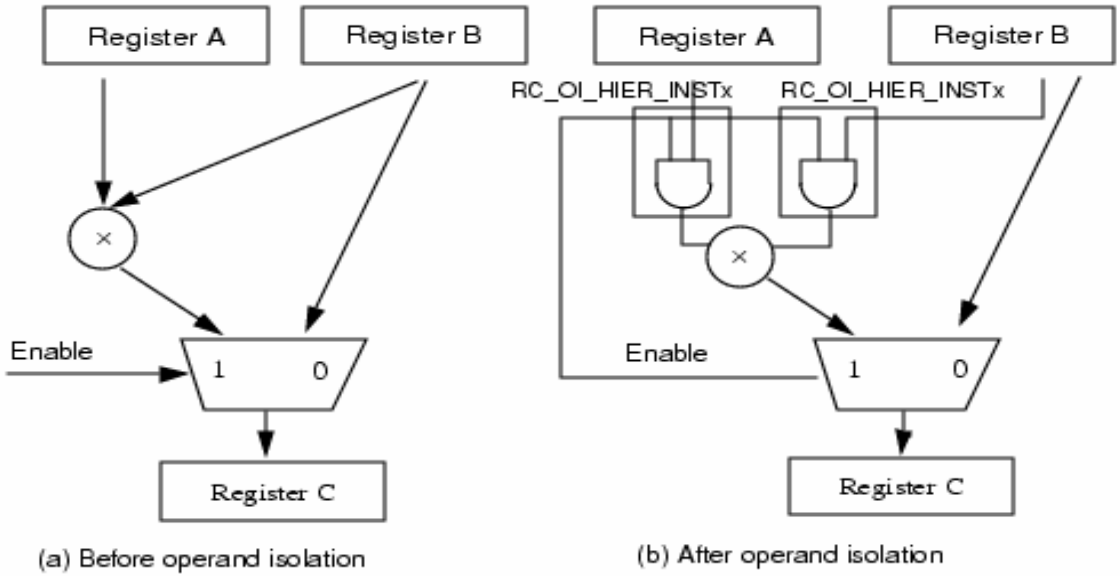
Operand Isolation

- Operand Isolation is a dynamic power optimization technique that can reduce power dissipation in datapath blocks controlled by an enable signal
- It can be done in RC using
  - set_attribute lp_insert_operand_isolation true



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Leakage Power Optimization

- Leakage Power can be reduced by using High V_T Cells which have lower leakage
- This can be done in RC using
  - set_attribute lp_multi_vt_optimization_effort low /

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MSV

Multiple supply voltages in a design is one of the most effective approaches to reduce the dynamic power dissipation of a design

- In RC
  - We use library domains to Indicate that some blocks in your design operate on different voltages
  - Associate dedicated libraries with some blocks in the design without using multiple supply voltages
- There are two types of MSV designs
  - Multiple Supply Single Voltage (MSSV): Core logic runs at a single voltage, but some portions of the logic are isolated on their own power supply. In this case isolation cells are required
  - Multiple Supply Multiple Voltage (MSMV): Supplies of different voltages are used for core logic. We have used MSMV in our design.In This case both isolation cells and level shifters may be required

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MSV

- A library domain is a collection of libraries that should have been characterized for the same nominal operating conditions
  - create_library_domain {$DOMAIN_1$ $DOMAIN_2$ … $DOMAIN_n$}
  - create_library_domain {DLXD IDD} (OUR CASE)
- Associating Libraries with voltage domain
  - set_attribute library {library1,library2} domain1
  - set_attribute library {library3} domain2
- Different blocks of your design may operate on different voltages
- To set the target library domain for the top design
  - set_attribute library_domain DOMAIN1 INSTANCE1
  - set_attribute library_domain DOMAIN2 INSTANCE2

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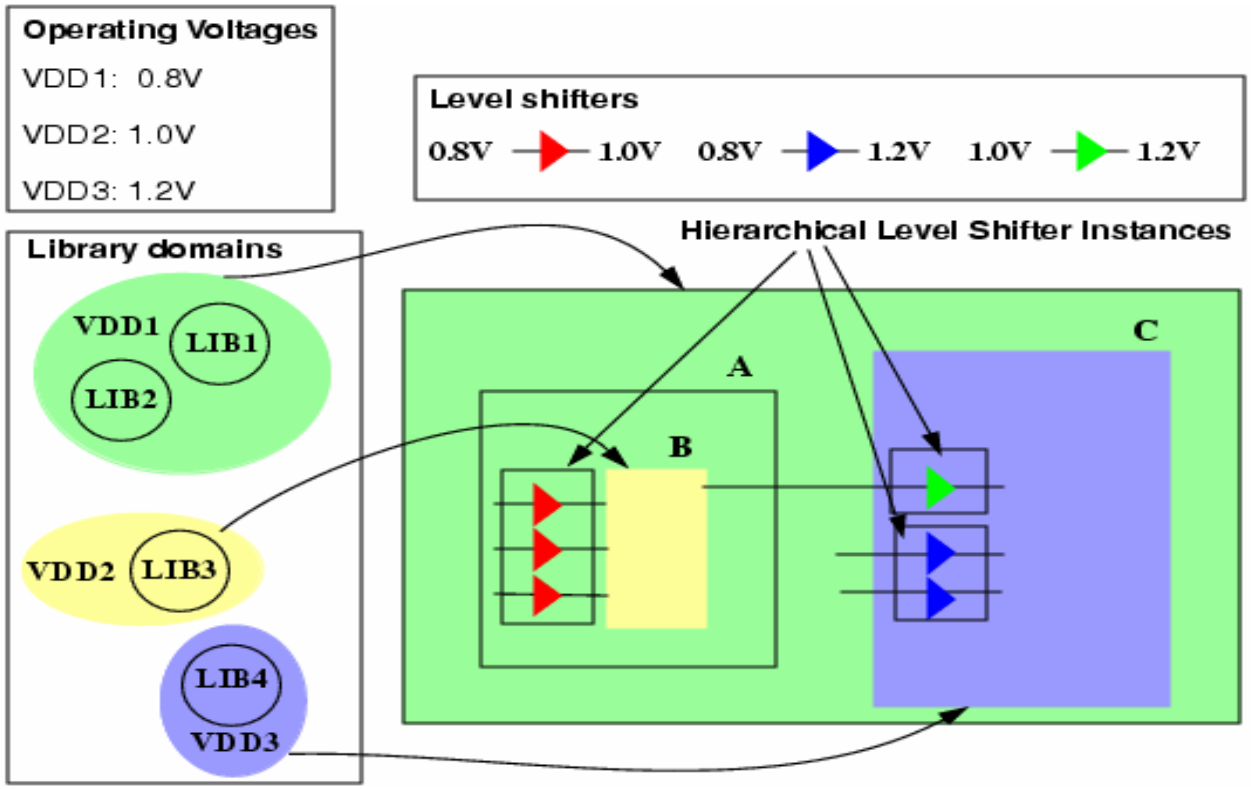
MSV



Partition of design into multiple voltage domains and communication between those domains

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Power Constraints

- Dynamic Power constraints can be specified in RC
  - set_attribute max_dynamic_power 2460 DLX_sync
  - 2460 is obtained from initial estimate of power that we did using RTL estimation
- Leakage Power constraints
  - set_attribute max_leakage_power 61 DLX_sync

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Low Power Synthesis Flow for DLX Processor Core

- read libraries
- set lp_auto_create_level_shifter 1
- create_library_domain {IDD DLXD}
- set_attribute library $1v0_lib_list IDD
- set_attribute library $0v8_lib_list DLXD
- set_attribute lp_insert_operand_isolation true
- read_rtl { ….}
- define_clock -name CLK -period 10000 [find / -port clk]
- set_attribute library_domain DLXD DLX_sync
- set_attribute library_domain IDD ID
- set_attribute max_leakage_power 61 DLX_sync
- set_attribute lp_multi_vt_optimization_effort low
- read_tcf design.tcf
- set_attribute max_dynamic_power 2460 DLX_sync
- set_attribute lp_auto_insert_level_shifter 1
- synthesize -to_generic
- synthesize -to_mapped
- clock_gating declone -hierarchical

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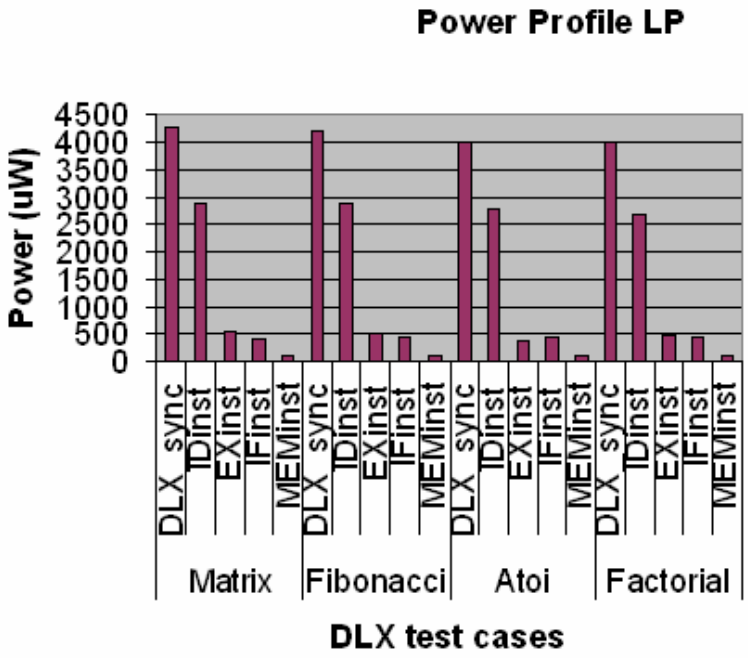
Low Power Synthesis Results

Wireload model

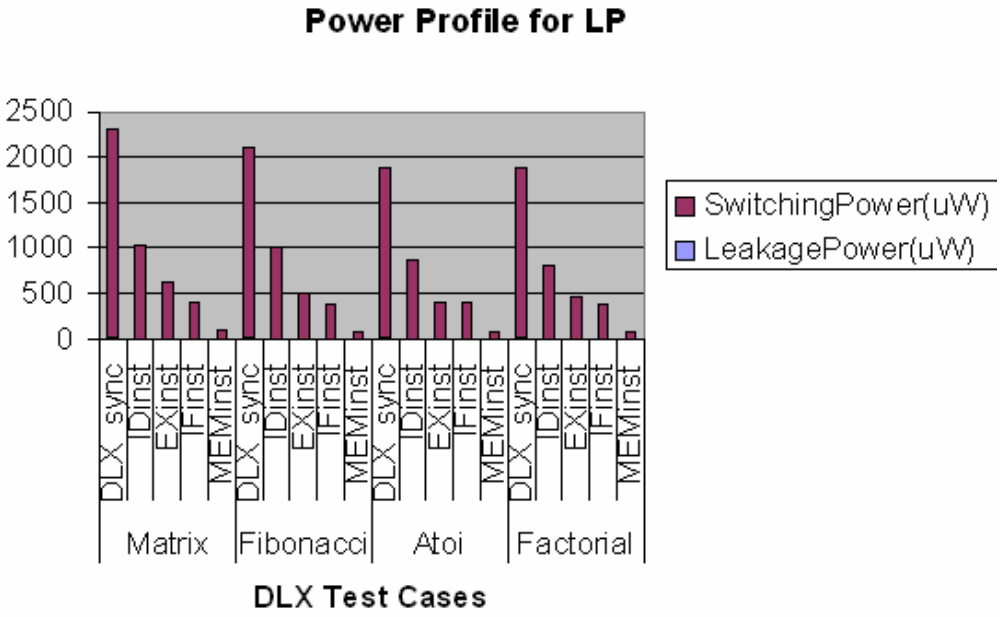
Original Testcase

Max Power: 4.28mW (matrix)



RTL Optimized Testcase

Max Power: 2.32mW (matrix)



Difference about ~46% to 53%!

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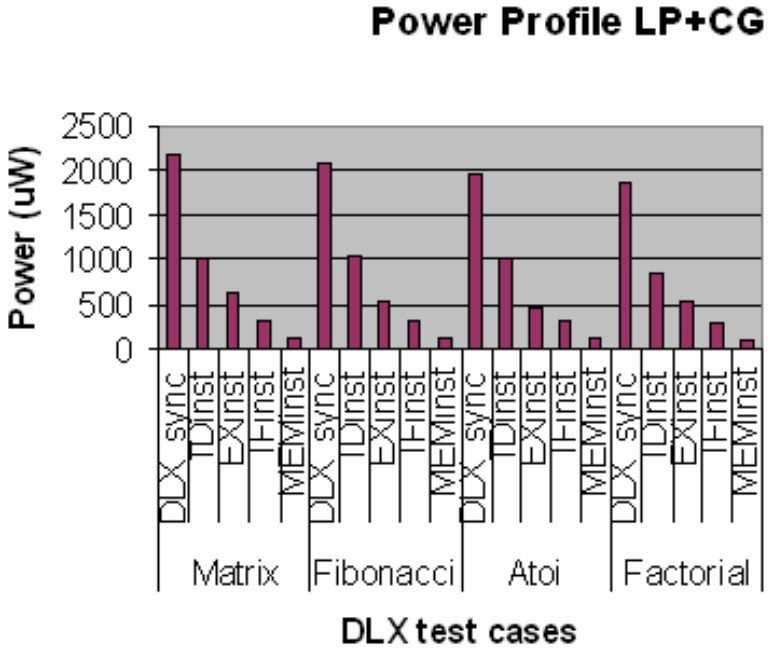
Low Power Synthesis Results

Wireload model

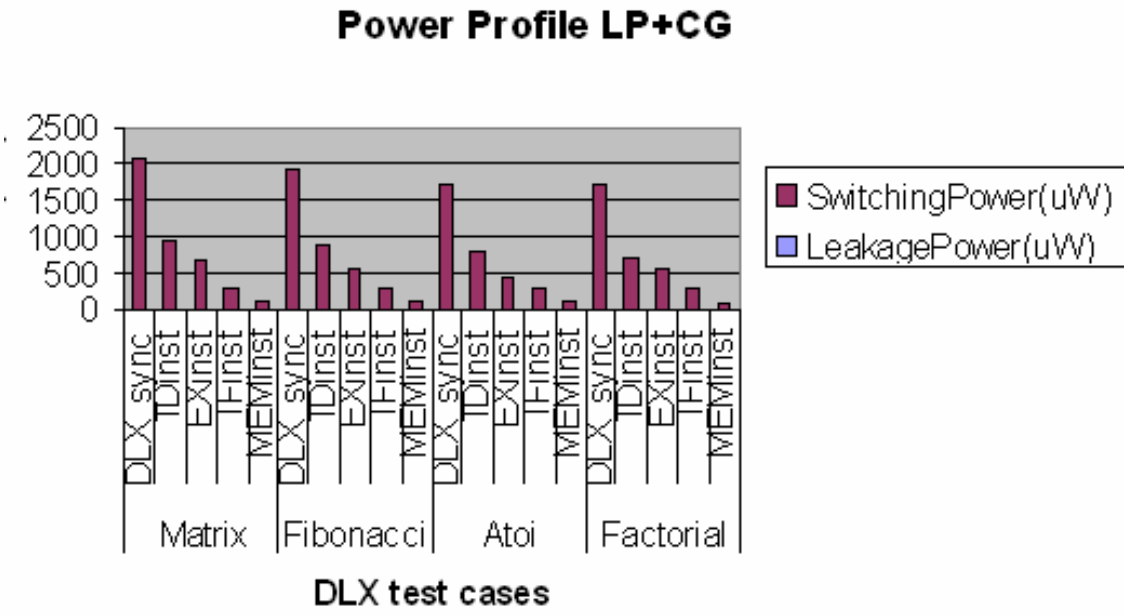
Original Testcase

Max Power: 2.16mW (matrix)



RTL Optimized Testcase

Max Power: 2.09mW (matrix)



Difference just ~3% to 8%!

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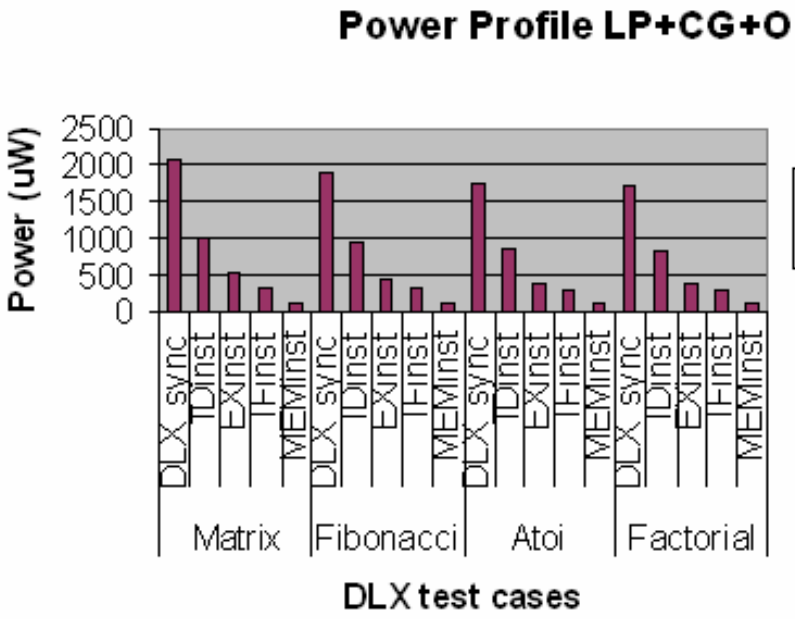
Low Power Synthesis Results

Wireload model

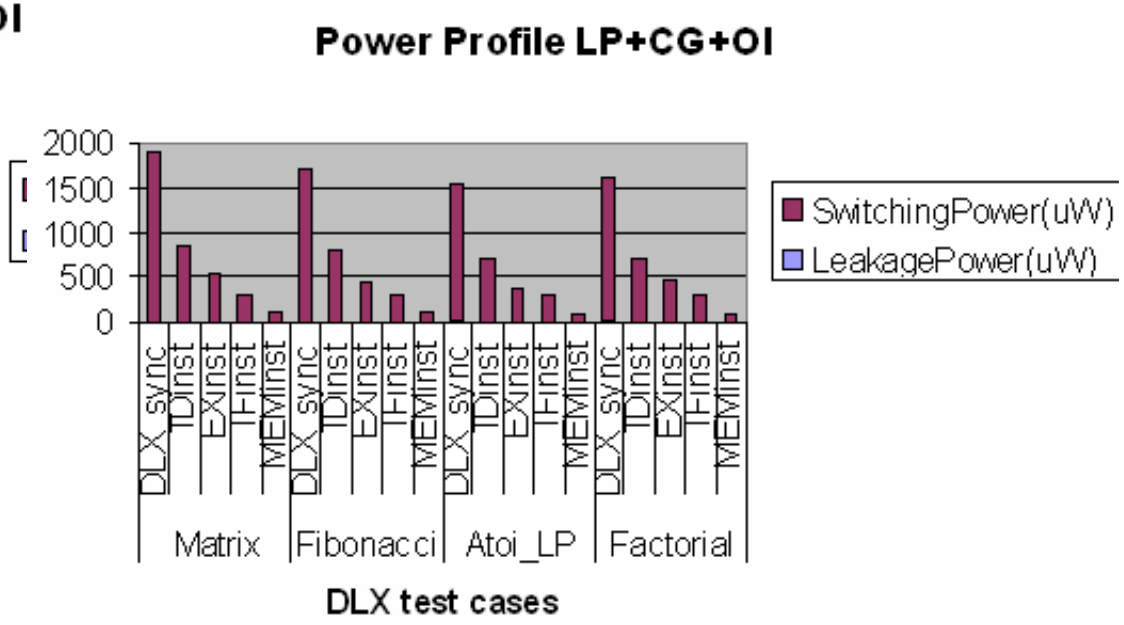
Original Testcase

Max Power: 2.08mW (matrix)



RTL Optimized Testcase

Max Power: 1.89mW (matrix)



Difference just ~5% to 9%!

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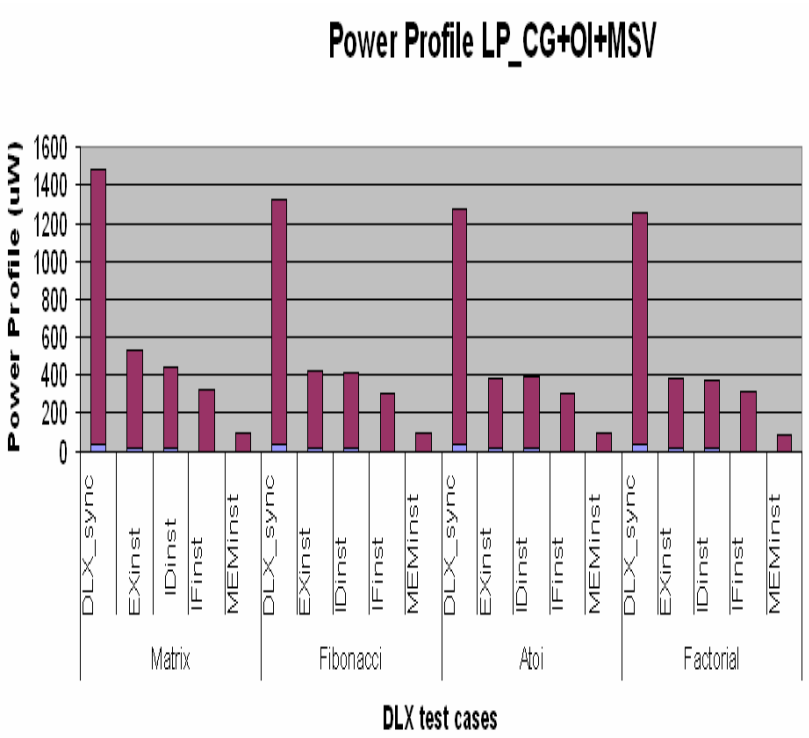
Low Power Synthesis Results

Wireload model

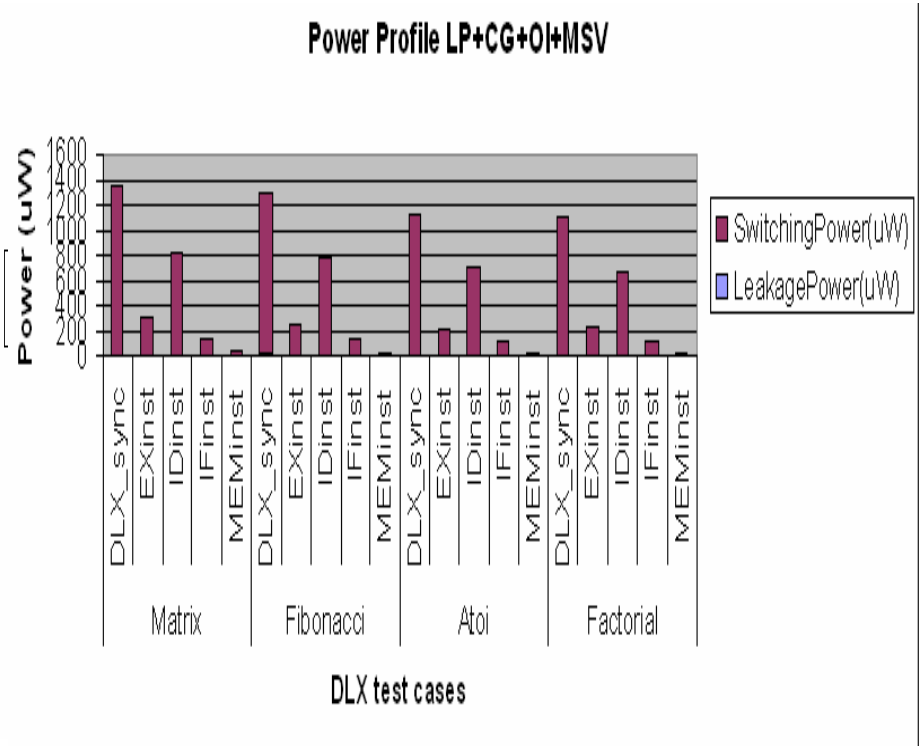
Original

Max Power: 1.48mW (matrix)



RTL Optimized

Max Power: 1.35mW (matrix)



Difference of ~3% to 12%! Max Switching = 1.35mW and leakage= 18.6uW
Reduction from Original baseline ~70%!!

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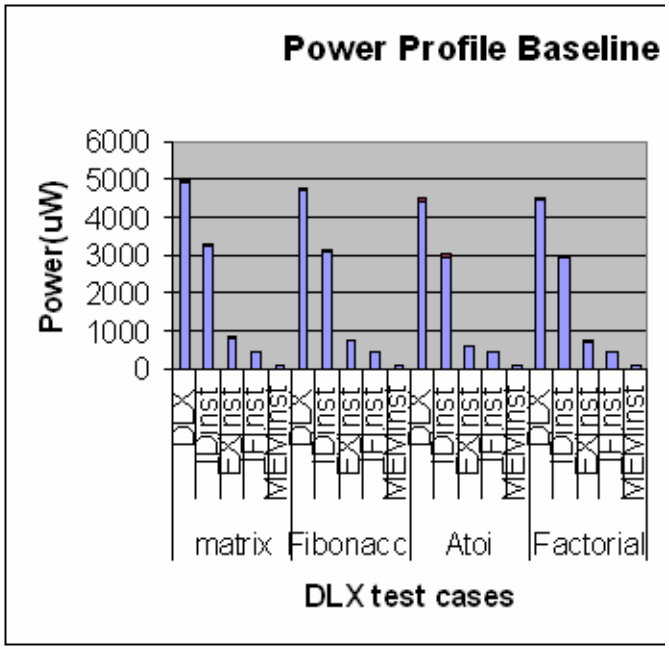
Low Power Synthesis Results

PLE model

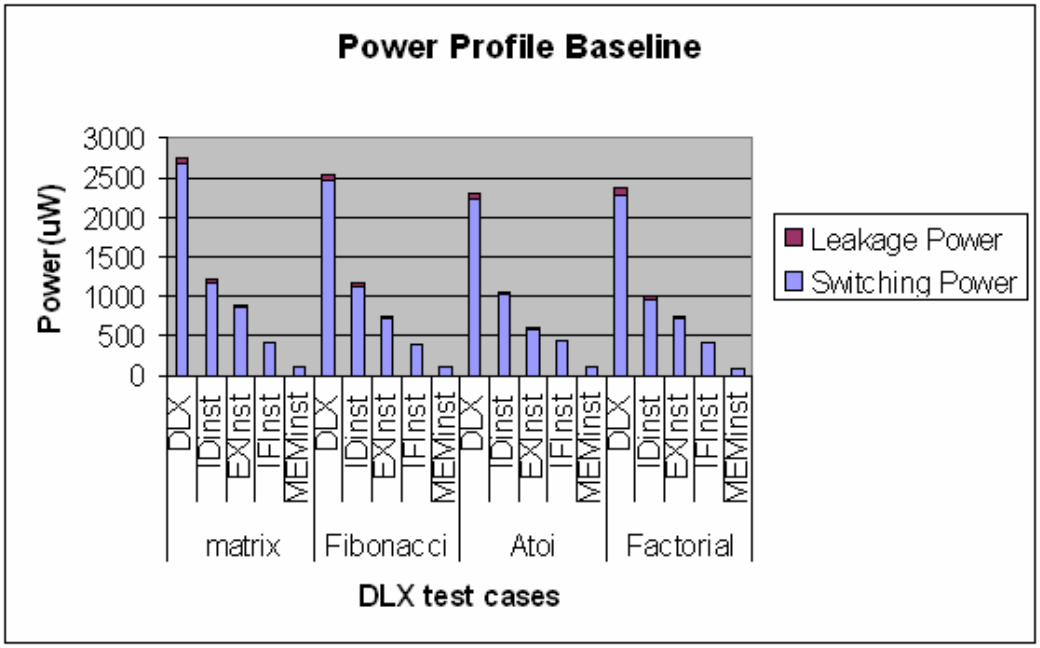
Original Testcase

Max Power: 4.99mW (matrix)



RTL Optimized Testcase

Max Power: 2.76mW (matrix)



Difference about ~48%!

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Low Power Synthesis Results

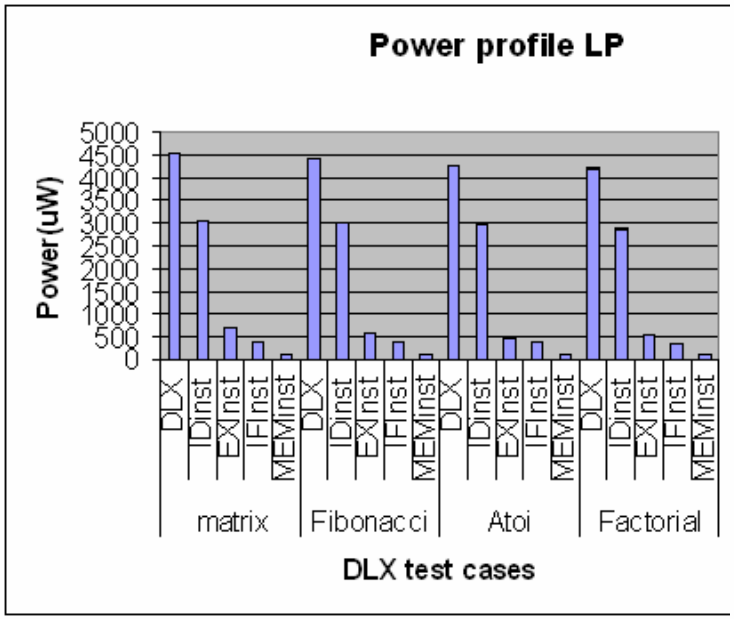
PLE model

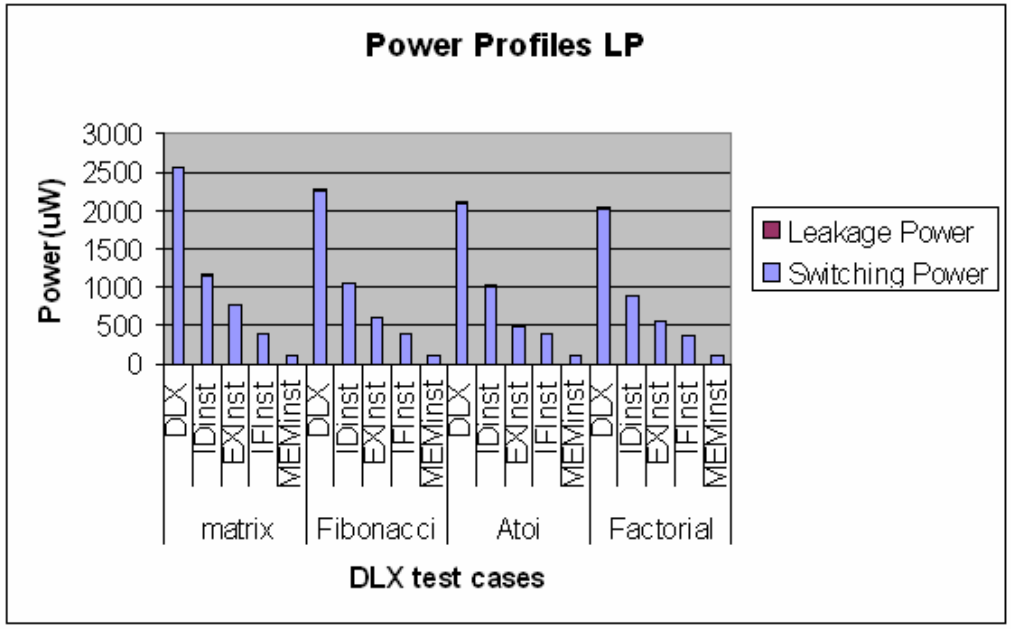
Original Testcase

Max Power: 4.55mW (matrix)

RTL Optimized Testcase

Max Power: 2.57mW (matrix)





Difference about ~44% to 52%!

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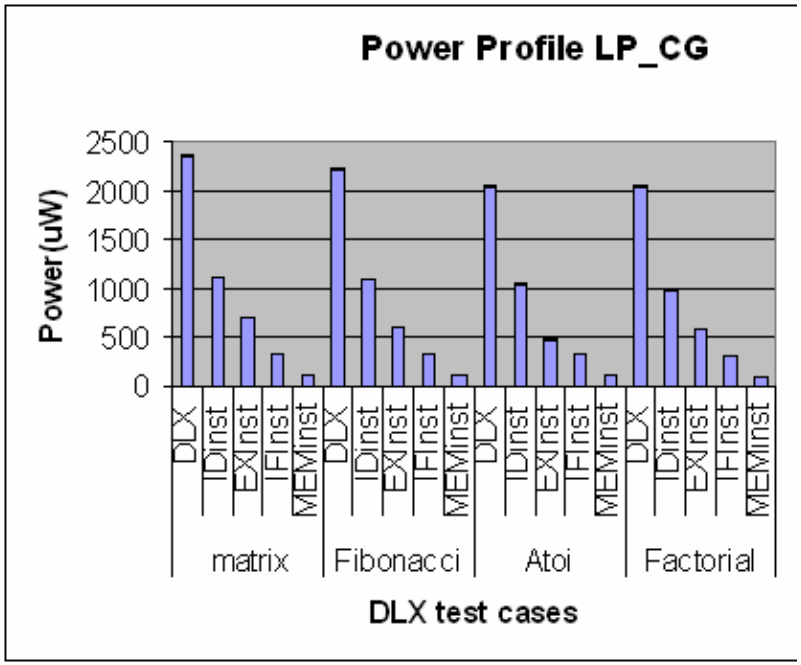
Low Power Synthesis Results

PLE model

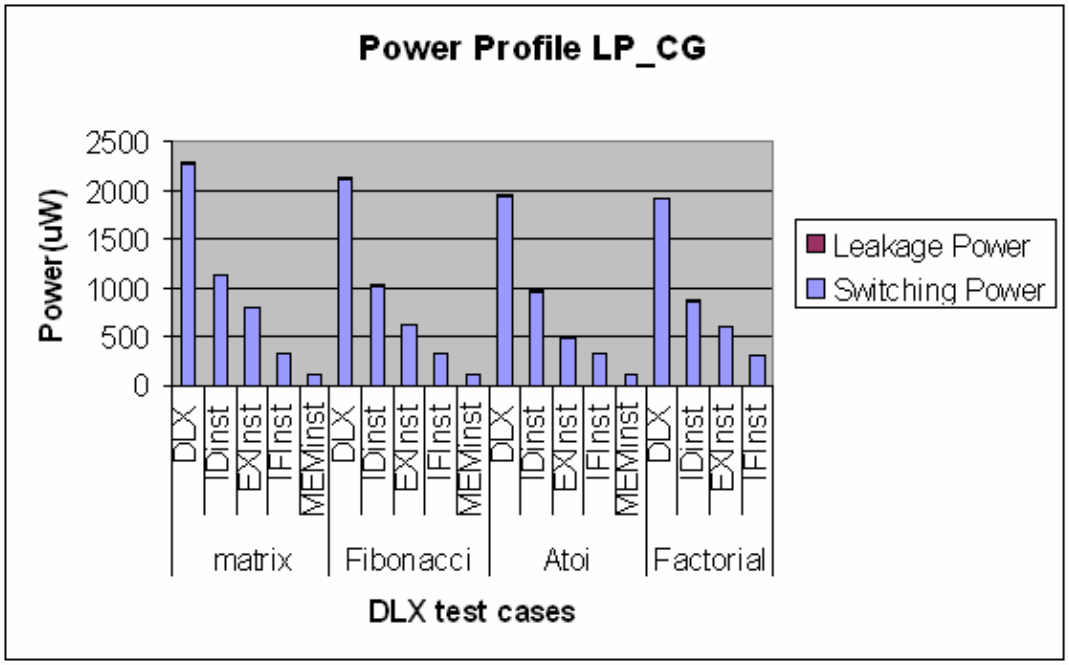
Original Testcase

Max Power: 2.37mW (matrix)



RTL Optimized Testcase

Max Power: 2.23mW (matrix)



Difference just ~3% to 7%!

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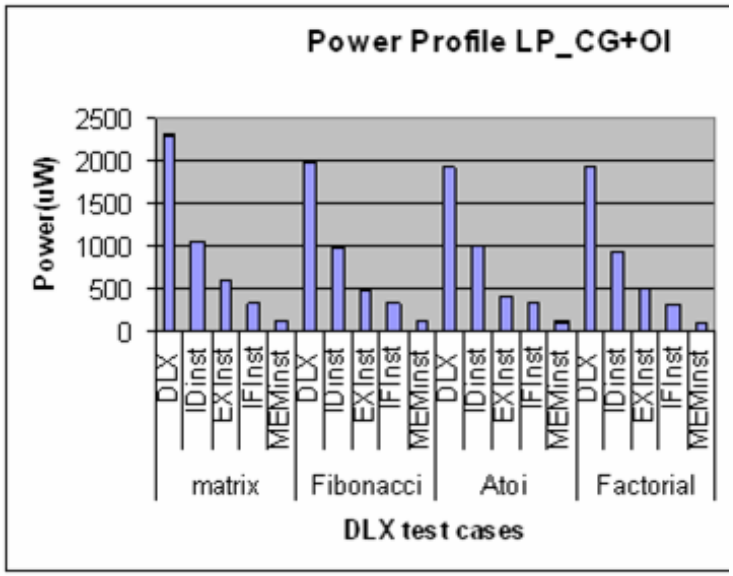
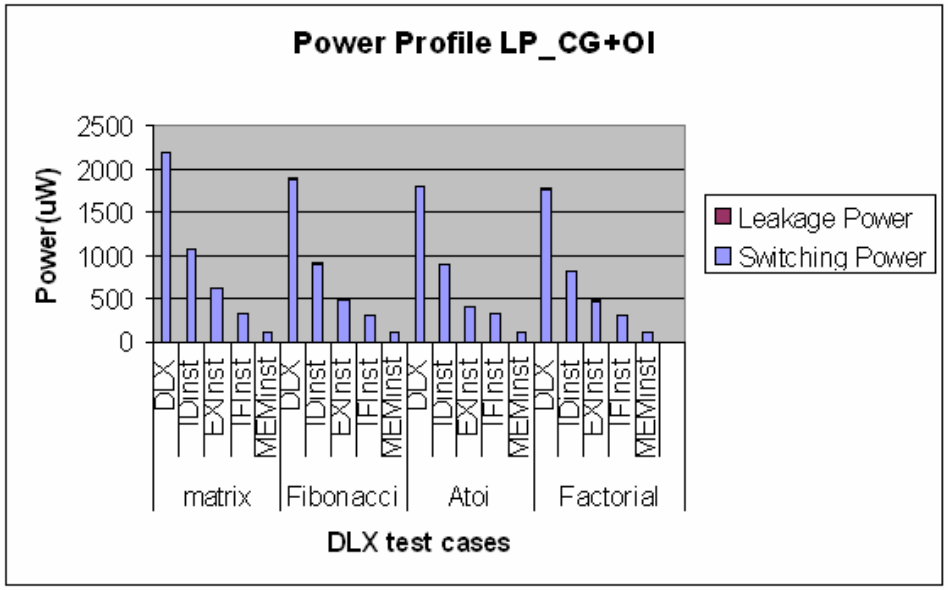
Low Power Synthesis Results

PLE model

Original Testcase
Max Power: 2.31mW (matrix)



RTL Optimized Testcase
Max Power: 2.2mW (matrix)



Difference just ~5% to 8%!

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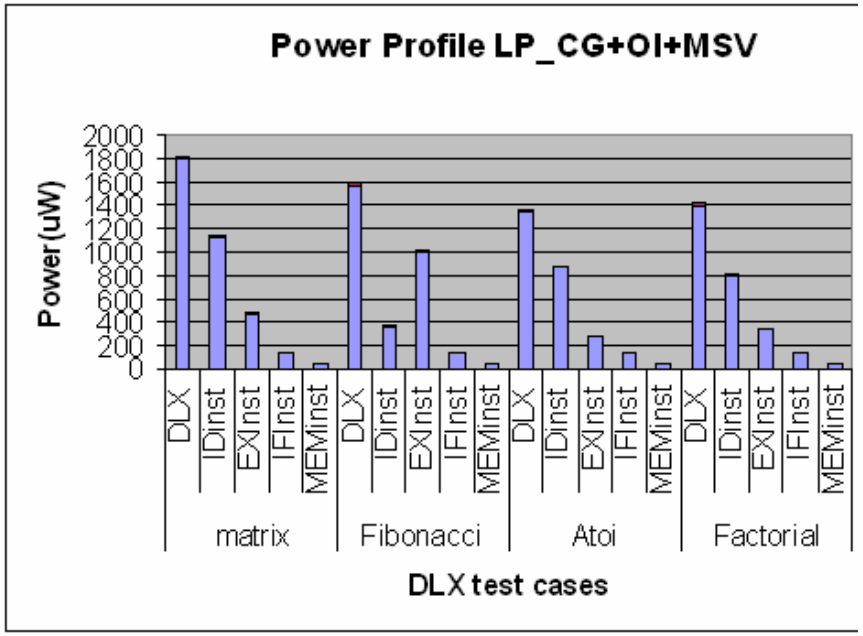
Low Power Synthesis Results

PLE model

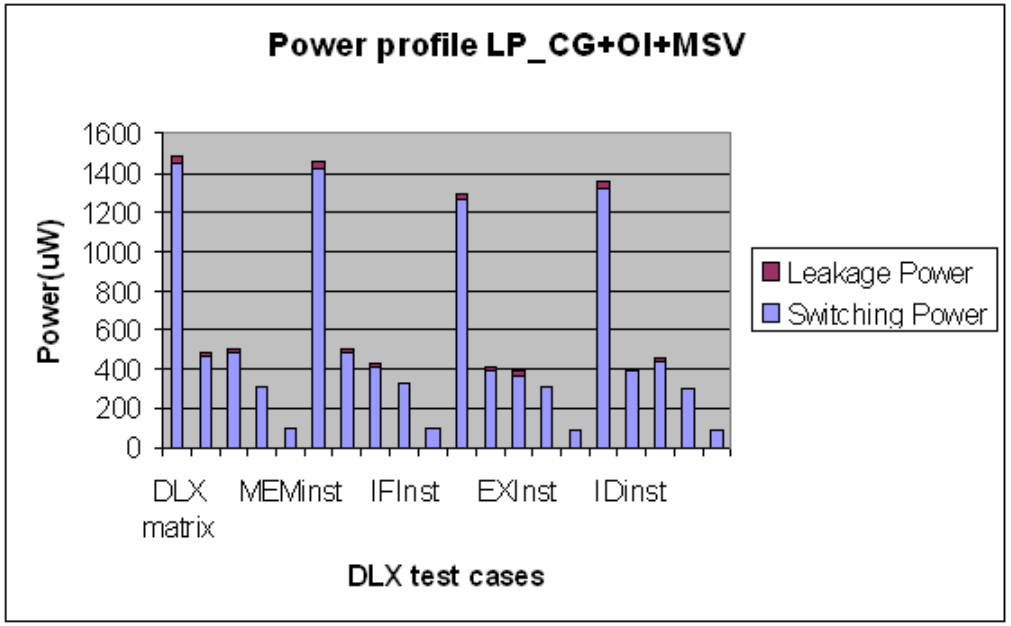
Original

Max Power: 1.83(matrix)



RTL Optimized

Max Power: 1.48mW (matrix)



Difference of ~5% to 19%!
From original baseline around 70% power reduction!

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Backend Flow

- Floorplanning Elements
  - Core Aspect: 1.0
  - Core utilization : 0.6
  - Power nets: VDD_DLXD (0.7V) and VDD_IDD(1.08V)
  - Ground net: VSS
  - Core ring: VDD_DLXD,VDD_IDD & VSS
  - IDD PD ring : VDD_DLXD, VDD_IDD & VSS
  - Power strips connect Core ring to IDD ring
  - Top & Bottom: M7, H ; Left & Right: M8, V
  - LVLLH and LVLHL Shifter cells

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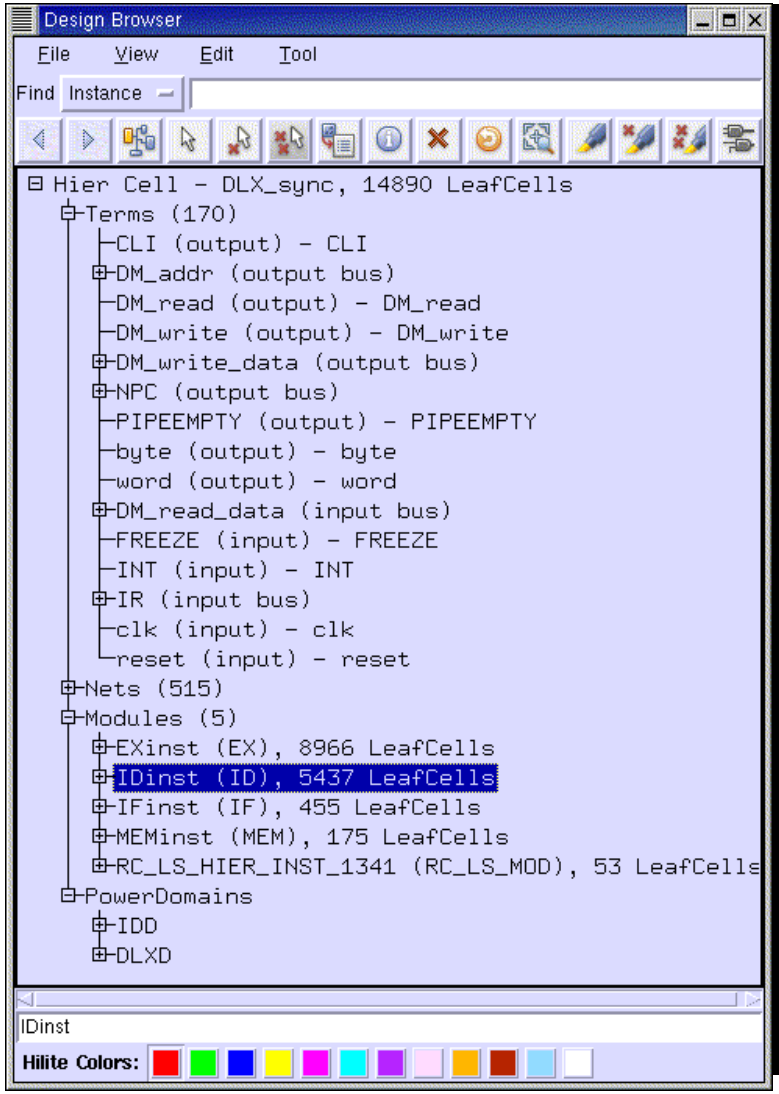
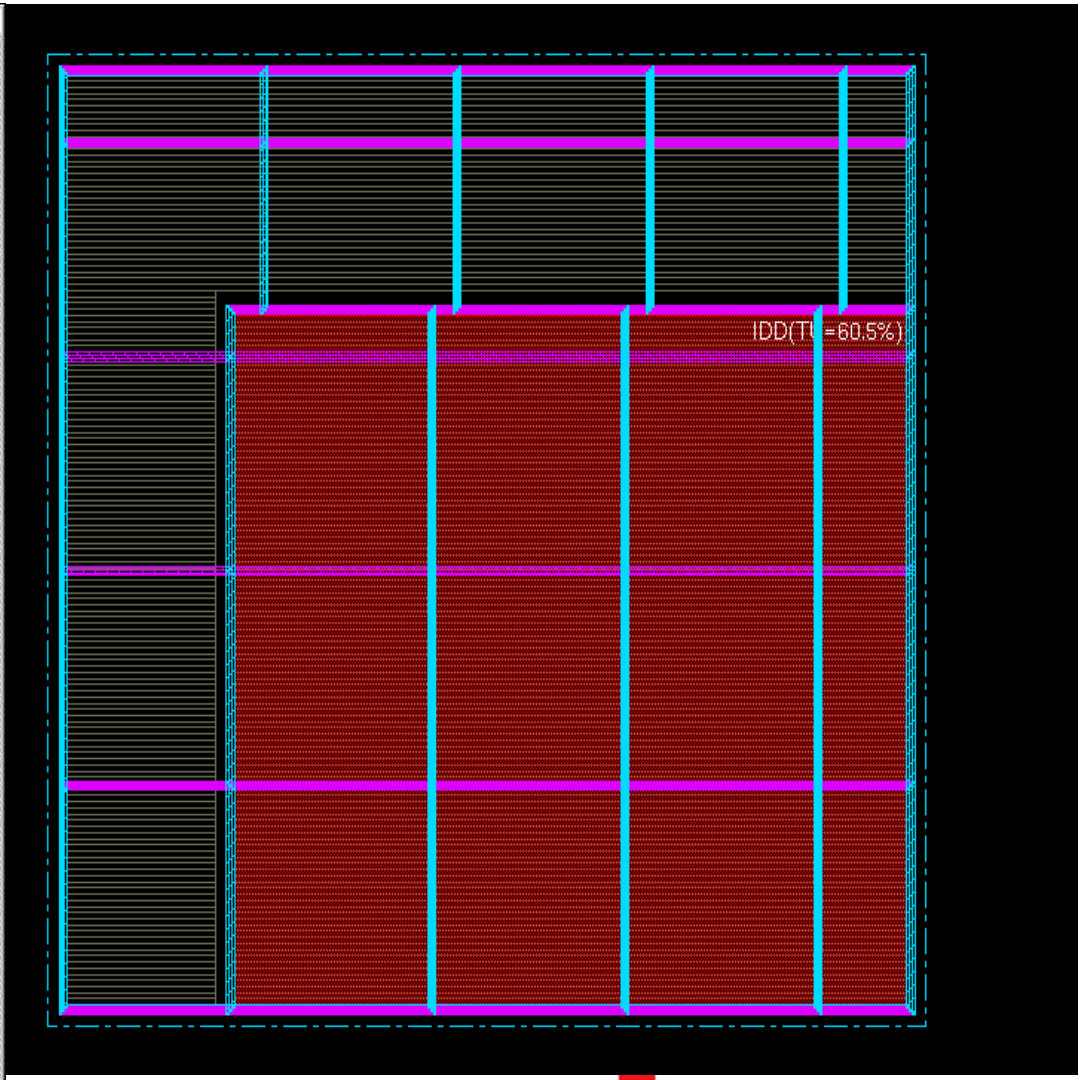
Power Planning





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Backend Flow

- Placement
  - Timing driven, Congestion Effort : High
  - In Place Optimization
- SRoute
  - DLXD
    - Std Cells – VDD_DLXD,VSS
    - Level Shifter Pins – VDD_IDD
  - IDD
    - Std Cells – VDD_IDD,VSS
    - Level Shifter Pins – VDD_DLXD
- PreCTS, PostCTS, PostRoute optimization

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Timing

- PreCTS Optimization
  - Density: 65.9%
  - Hold: 0.013ns (WNS)
  - Setup: 1.1ns (WNS)
- PostCTS Optimization
  - Density: 66.8%
  - Hold: 0.962ns (WNS)
  - Setup: 1.108ns (WNS)
- PostRoute Optimization
  - Density: 71.1%
  - Hold: 1.016ns (WNS)
  - Setup: 0.697ns (WNS)

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Power Outcome

- Total Power after PnR (Comb: 60%, Seq=40%)
  - Total Internal Power: 1.38mW
  - Total Switching Power: 0.77mW
  - Total Leakage Power: 65.084 uW
  - Total Total Power: 2.22 mW
  - DLXD: 36.5%, IDD: 63.5%
- Clock Power distribution (19.39% of total power)
  - Internal: 173.22uW
  - Switching: 255.887uW
  - Leakage: 2.05uW
- Fibo baseline: 4.78mW; Fibo Layout: 2.22mW
  - Reduction: 53.5%

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Conclusion

- DLX Processor Core's pipelined structure
- RTL Level Power Estimation Methodology
- ID's register file consumed max power so redesigned it
- RTL redesign helps reduced power by 70%!!
- Testcases face varied effects of LP,CG,OI,MSV
  - For seq dominated, CG helps a lot!
- Max. power reduction effect in Synthesis
- Completed Front End and Back End flow
- RTL estimated 36% less power mainly due to optDesign

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THANK YOU!

Q &A

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