SUCCESS STORY

CADENCE AND NEMERIX

NemeriX Partners with Cadence VCAD Engineering Services Team to Meet Aggressive Power and Performance Goals for Next-Generation GPS Baseband IC

"Our partnership with Cadence VCAD Engineering Services continues to be a very important element in our success. It allows us to extend our design team beyond our own employees, and no one is willing to settle for anything less than best in class for both our power and performance goals."

Gianmaria Mazzucchelli, *Vice President of Engineering, NemeriX*

CORPORATE PROFILE

- NemeriX creates ultra-low-power RF and baseband ICs for GPS and wireless applications

DESIGN CHALLENGE

- Achieve the lowest possible power consumption for new GPS chipset
- Complete back-end process for complex design in two months

CADENCE SOLUTION

- Deployed the Cadence Encounter® digital IC design platform low-power flow using Virage ultra-high-density (UHD) libraries to address both front- and back-end design challenges
- Trained NemeriX engineering team on best practices for future designs

CADENCE PRODUCTS AND SERVICES

- Cadence VCAD Engineering Services
- Cadence Encounter digital IC design platform

GLOBAL LOCATION DETERMINATION ANYWHERE, ANYTIME

Based in Manno, Switzerland, NemeriX is a fabless semiconductor company delivering the world's lowest power global positioning system (GPS) chipsets for both indoor and outdoor applications. The global market potential for efficient mobile GPS technology is significant for applications ranging from wireless phones and PDAs to mobile emergency systems, however low system cost and small size are critical to accelerating technology adoption.

The NemeriX design team was beginning work on the NJ2020, their next-generation ultra-low-power baseband processor for indoor assisted GPS and enhanced performance stand alone GPS applications. "Our goal was to deliver the smallest package operating at the lowest power with tracking sensitivity, acquisition time, and accuracy equal to or better than the competition," said Gianmaria Mazzucchelli, vice president of engineering at NemeriX. "In other words, the user would have all the performance they expect, but in a much smaller device with the longest available battery life."

MULTI-DISCIPLINARY DESIGN APPROACH, LOW-POWER METHODOLOGY

In order to achieve the lowest possible power consumption in their designs, NemeriX has adopted a unique, group design approach. "We take a 'multi-disciplinary' approach to our designs," said Mazzucchelli. "What this means is that our systemlevel software guys, our hardware team, and our layout engineers all work closely together to create optimal partitioning for the hardware and software. They work as a unit to optimize power management and clock management of all the devices on the chip." With the design team working as one, NemeriX needed to find a new lowpower methodology to meet their performance goals. "We have a successful partnership with the Cadence VCAD

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>
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Engineering Services team that goes back a few years," continued Mazzucchelli. "This time, we called on them to help us adopt a new set of design tools to meet our low-power challenge."

ENCOUNTER LOW-POWER DESIGN FLOW ENABLES ADVANCED OPTIMIZATION TECHNIQUES

The NJ2020 design presented significant challenges, particularly in the areas of power grid and clock tree insertion and optimization. "We designed the chip so that the power domains and clock frequencies could be dynamically adjusted as a function of the activity of the chip," said Mazzucchelli. "This means that approximately 10% of the circuitry is in 'always on' mode, and the needed parts of the remaining 90% are turned on only when necessary." To do this, the team had to partition the digital portion of the design into more than four different power and clock domains over the chip.

To address these challenges, the Cadence VCAD Engineering Services team deployed the Encounter lowpower design flow, which automatically supports a multiple power domain methodology. Nemerix selected the Virage Logic ASAP Logic™ Ultra-High-Density (UHD) standard cell libraries and ASAP Memory instances targeting TSMC 130nm technology for their low-power consumption and integration with the Cadence Encounter low-power design flow. "Cadence VCAD seamlessly introduced the Encounter platform into our design flow to address both front- and backend design issues that arose in our quest for ultra-low power," continued Mazzucchelli. "They showed us how to leverage complex techniques such as multiple supply voltage and multiple voltage library optimization, saving us significant time while improving our results."

NEMERIX LEVERAGES THE ENCOUNTER PLATFORM TO MEET TIGHT SCHEDULE

The NemeriX team had only two months to complete the back end of the NJ2020 design. "We were faced with an aggressive time line for this part of our design," said Mazzucchelli. "Again, the Cadence VCAD team had the right answer with the Encounter platform." The VCAD team used advanced technologies in the Encounter platform to perform detailed routing, parasitic extraction, crosstalk analysis, IR drop analysis, timing optimization, static timing analysis, and layout vs. schematic/design rule checking on the design.

"The work that the Cadence VCAD team performed on the back end of the NJ2020 design enabled us to deliver the GDSII to TSMC on time, meeting all of our specifications," said Mazzucchelli. "Importantly, during every step of the process, the Cadence VCAD team made recommendations and taught our engineers how to maximize results for each task, creating scripts and procedures to reference on our next design."

As a result of this collaboration, NemeriX produced the world's lowest power indoor GPS baseband processor, consuming less than 50mW. When the NJ2020 is combined with the NemeriX NJ1006A GPS receiver, the resulting power consumption is 70% lower than competitive offerings.

CONTINUING A SUCCESSFUL PARTNERSHIP

Over the past few years, the NemeriX and Cadence VCAD teams have partnered on several projects. "Our partnership with Cadence VCAD Engineering Services continues to be a very important element in our success," said Mazzucchelli. "It allows us to extend our design team beyond our own employees, and no one is willing to settle for anything less than best in class for both our power and performance goals."

"We are very pleased with the technical contributions from the Cadence VCAD team with their Encounter technology and the Virage Logic low power IP solutions," said Ron Torten, chief executive officer at NemeriX. "The design methodology that we were able to create inside NemeriX enabled us to achieve first silicon success and meet a critical market window."

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Success Story Reference NemeriX 07/06
20644