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Quantus QRC Extraction Solution

Next-generation tool with 5X better performance and scalability, best-in-class accuracy, and in-design and signoff parasitic extraction

Cadence® Quantus™ QRC Extraction Solution is a next-generation parasitic extraction tool for digital and custom analog flows. Providing up to 5X better performance than competitive products, the tool features massively parallel architecture for fastest performance and scalability across hundreds of CPUs. Its high-accuracy modeling engine has been significantly enhanced to support FinFET designs and uses the same foundry-qualified "qrctechfiles" for digital and transistor extraction. The solution, employing a robust 3D modeling framework, is fully certified for the 16nm FinFET process at TSMC.

Overview

As advanced process geometries continue to shrink, parasitic extraction has become critical throughout the design implementation flow and the signoff phase. Quantus QRC Extraction Solution is a production-proven signoff extraction tool ideal for advanced nodes, including FinFET designs. The solution, which includes an integrated, random-walk field solver, Quantus FS, models physical effects to ensure that extracted parasitics match those on silicon. Developed with massively parallel architecture, the tool performs up to 5X better than competitive products. By delivering higher accuracy parasitics, the tool helps you to reduce overall design cycle times and significantly enhances the quality of silicon in complex designs.

Integrated with the Cadence Virtuoso® custom design platform and the Cadence Encounter® digital implementation platform, Quantus QRC Extraction Solution is the most complete and efficient path to accurate parasitic extraction for all mainstream and advanced node designs, including FinFET.

Key Benefits

- Better accuracy for FinFET designs versus foundry golden
- Tighter accuracy against field solver, with a near-zero mean
- Highly accurate critical nets extraction with integrated field solver technology
- High performance and scalability with massively parallel architecture, supporting a linear gain when the number of CPUs used is doubled
- Scalability for single- and multi-corner extraction runs, with 2X to 3X faster performance in multi-corner runs
- Better signoff turnaround time (TAT) at the chip finishing level via automated incremental extraction, delivering an additional 3X better performance
- Unmatched accuracy and a significantly reduced netlist that enables faster simulation and characterization runtimes for FinFET designs
- Extracted View enables easy and efficient simulation with Virtuoso Analog Design Environment
- Faster and better design convergence with integration with Virtuoso Analog Design Environment and Cadence Encounter Digital Implementation System
- Inductance extraction for LEF/DEF flow enables highly accurate analysis of CLK nets for 28nm and below designs

Features

Massively parallel technology

Quantus QRC Extraction Solution is built with massively parallel technology to extract multi-million gate chips efficiently. The extraction tasks are distributed across multiple CPUs and/or machines for execution in parallel. As a result, the tool, which scales easily to hundreds of CPUs, can deliver a linear performance gain when the number of CPUs used is doubled.

Multi-corner/temperature extraction

With the exploding number of process corners at advanced nodes, design convergence is becoming a bottleneck in the design flow process. For example, signal integrity issues

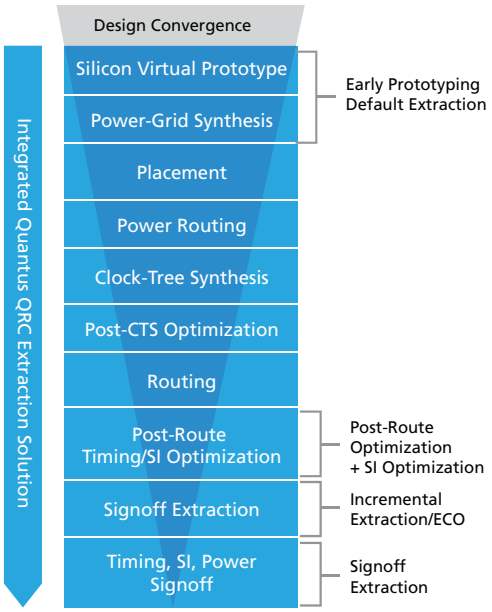


Figure 1: Enabling in-design in the Encounter digital implementation platform

can occur at high-temperature conditions, requiring efficient multi-corner extraction performance including temperature corners. Quantus QRC Extraction Solution extracts multiple corners simultaneously while significantly reducing overall runtime without compromising on accuracy. In fact, the tool delivers 3X faster performance in multi-corner runs vs. single-corner runs done in parallel.

Support for 16nm FinFET processes

Quantus QRC Extraction Solution is fully certified for the 16nm FinFET process at TSMC. The FinFET process introduces additional parasitic challenges in capacitance and resistance. Benchmark tests have demonstrated that the tool offers unmatched accuracy vs. the foundry golden. Compared to competitive solutions, the tool also delivers 2.5X faster netlist simulation runtime with a 2X smaller netlist, and faster characterization of standard cells, SRAMs, and IP.

Advanced substrate modeling capability

RF designers need a tool that extracts parasitic inductance accurately and also evaluates the impact of substrate parasitics on their designs. Substrate noise coupling is a growing concern due to higher frequencies, higher integration, smaller feature sizes, and lower supply voltages. Including the p-substrate and n-well as part of the substrate model affects the extract result and leads to RF interconnect loss. Quantus QRC Extraction Solution includes a full 3D substrate model with full-chip and block-level views for accurate simulation and analysis of RF IC circuits, and equips you to perform what-if analysis for substrate noise distribution.

Better design convergence via integration with Virtuoso and Encounter platforms

As an integral part of the silicon analysis function inside the Virtuoso custom design platform, Quantus QRC Extraction Solution provides critical parasitic information for optimizing chip performance and yield. Essentially, the extraction tool brings the physics of interconnect parasitics into the Virtuoso environment for designing, characterizing, and optimizing chip layouts.

Through the tool's integration with the Encounter Digital Implementation System, you benefit from a seamless solution for timing, IR, electromigration (EM), signal integrity analysis, and power verification. Used in-design with the Encounter environment, Quantus QRC Extraction Solution equips you to reduce design turnaround time by performing incremental extraction, and to reach timing closure faster by using signoff-accurate extraction data for timing and noise optimization.

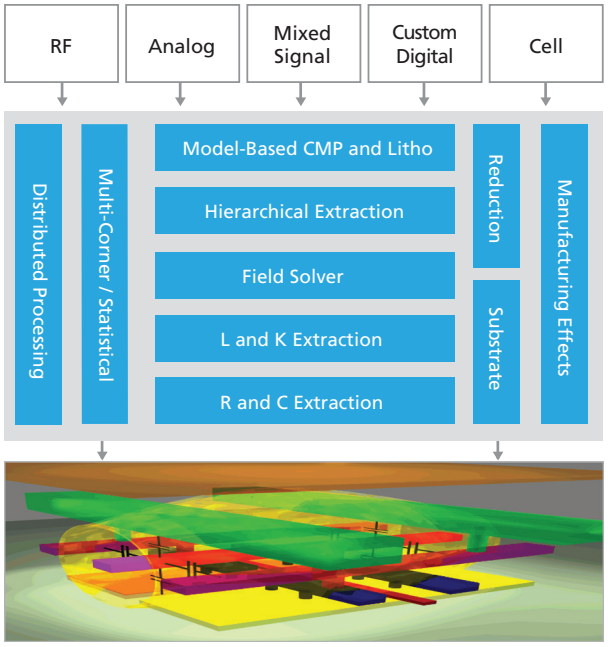


Figure 2: Key functionalities of Quantus QRC Extraction Solution

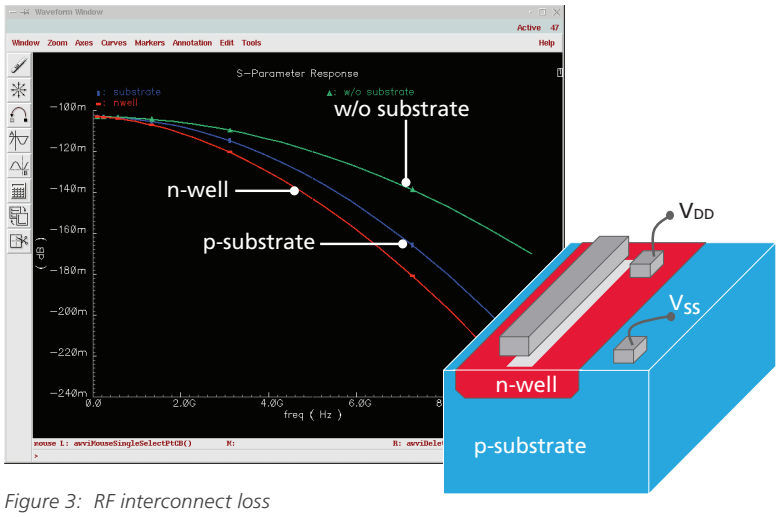


Figure 3: RF interconnect loss

Binary interface with Tempus Timing Signoff Solution

At advanced nodes with multi-million instance designs, it's critical to prevent parasitic load, read, and analysis turnaround time from becoming a bottleneck. Quantus QRC Extraction Solution provides a binary interface and format, RCDB, with Cadence Tempus™ Timing Solution and Encounter Digital Implementation System. RCDB is a random-access format that reduces memory footprint. The format offers up to 120X better performance while reading in the SPEF file into Encounter Timing System, and 3X overall runtime performance improvement for extraction and SPEF read times, with no compromise on accuracy.

Support for all design types

With its built-in, advanced functionality, Quantus QRC Extraction Solution supports all design types including: custom/analog and RF, SerDes, IP/SRAM/bitcell characterization, memory, Power MOSFETs, and image sensors. Capabilities enabling this support include:

- Substrate noise analysis
- Inductance extraction for both GDS and LEF/DEF flows
- MeshR including adaptive meshing technique
- RCLK reduction

Specifications

Packaging

- Available in L and XL configurations for basic extraction

Foundry

- Quantus QRC Extraction Solution process files are:
  - Certified and supported by TSMC
  - Flow tested and qualified with foundry process design kits (PDKs)
  - Complemented by development services (available from Cadence)

Format support

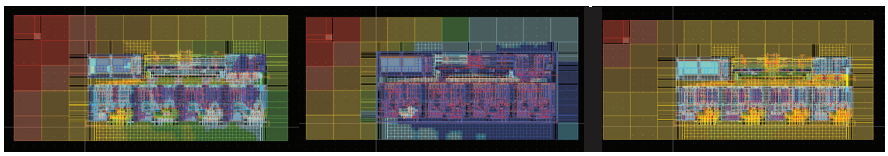
- Design input: GDSII, LEF/DEF, DFII, OA
- LVS data from Cadence Assura® Physical Verification, Cadence Physical Verification System, and Mentor Graphics Calibre platform
- Design output: Extracted View, DSPF, xDSPF, SPICE, SPEF, xSPEF, SSPEF
- Direct binary interface to Tempus Timing Signoff Solution—RCDB

Platforms

- IBM AIX (64 bit)
- Linux (32 bit, 64 bit)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more



Lightly doped substrate, no guard ring

Lightly doped substrate with guard ring connected to ideal power supply

Heavily doped substrate, no guard ring

Figure 4: What-if analysis with noise contour map

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