cādence®

Assura Physical Verification
Design rule checking and layout vs. schematic verification

Cadence® Assura® Physical Verification—a key component of the design verification suite of tools within the Cadence Virtuoso® Custom Design Platform—is the physical verification solution of choice for AMS/custom designers. It utilizes hierarchical processing and multiprocessing for fast, efficient verification in both interactive and batch mode.

Assura Physical Verification

Assura Physical Verification forms a key component of the design, parasitic extraction and simulation flow within the Virtuoso Custom Design Platform. As a trusted solution with many hundreds of users worldwide, it enables design teams to check, identify, and correct design and connectivity errors to achieve design sign-off before tape-out.

The technology uses hierarchical processing and multiprocessing techniques to rapidly facilitate accurate identification and correction of design rule errors in even the most advanced designs. With its GUI-guided debugging environment, Assura Physical Verification accelerates the debug and rework cycle and so reduces overall verification cycle time. Assura Physical Verification provides the best choice for fast and silicon-accurate analysis of custom, AMS, and RF IC designs and IP blocks.

Benefits

- Trusted solution with hundreds of users worldwide

- Key component of Virtuoso physical design and simulation platform

- Intuitive and powerful debug environment based on Virtuoso platform accelerates check/rework cycle

- Seamless integration with Cadence QRC transistor-based parasitic extraction and simulation flow gives fast, silicon-accurate analysis

- Advanced design rule capabilities facilitate nanometer process checks

Features

Unified Design, Verification, and Analysis Environment

Assura Physical Verification is an integral part of the Virtuoso Custom Design Platform. Every release of Assura Physical Verification is flow tested with the other platform components. The resulting unified environment accelerates custom design, verification, analysis, and simulation leading to increased design productivity, chip performance, and silicon yield.

Performance and capacity

Assura Physical Verification uses hierarchical processing and multipro-cessor techniques to increase perfor-mance and capacity. Assura Physical Verification efficiently processes highly repetitive structures (such as memory) with its hierarchical processing techniques. A hierarchical debugging capability further accelerates the debug cycle because multiple instances of errors in the same hierarchy only have to be corrected once. Finally, multiprocessing increases design throughput by leveraging cost-effective and ubiquitous multi-CPU hardware.

Interactive and batch verification

Assura Physical Verification supports runs in interactive and batch mode. Interactive physical verification integrated within the Virtuoso Custom Design Platform helps designers to maximize silicon performance and yield in hand-crafted, full custom IP. Designers can then script and run Assura Physical Verification in batch mode once the custom IP blocks are assembled as a finished chip. A single rule file supports both interactive and batch verification modes.

Electrical rule checks

A comprehensive set of electrical rule check (ERC) commands verifies that designs conform to connection, tracing, and specific connectivity properties that are established for a given fabrication process or process variant.

Assura Physical Verification provides full set of ERC capabilities, including:

• External Connection Definition Rules

• Path Tracing Rules

• Nonfunctional Device Checking Rules

• Specific Connectivity

• Debug GUI support for ERC

Unique pattern checking capability

Certain advanced checks, such as metal enclosure of contact at line-end, are not easy to write and are best checked using pattern recognition methods. Assura Physical Verification incorporates unique pattern checking capabilities to accelerate advanced rule development and maintenance for checks that would be difficult to write using traditional approaches. This approach can provide up to 20x performance improvement for advanced checks, which in turn can improve the overall run-time for the entire DRC task by up to 2x.

Density check and metal fill

Assura Physical Verification offers context-sensitive fill patterns, meaning users can place whatever patterns wherever they are needed in the layout. Users can customize fill patterns and shapes (e.g., custom fill cells, squares, rectangles, skewed, bridging bars) as necessary
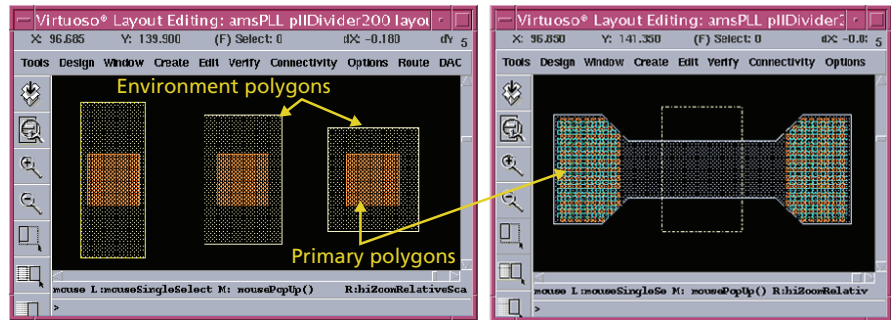

Figure 1: A set of design rules are described by drawings in a model file (GDSII, DFII, text vertices). A model contains a primary polygon (e.g., contact, fuse opening, DRC error markers) and environment polygons (e.g., metals enclosing contact, fuse metals/vias, waivable layout configuration per error marker). Pattern check is triggered by primary polygons in the design.

to balance layout density. The area fill command is also capable of connecting area fill features. Assura Physical Verification can perform area fill in flat or hierarchical mode.

GUI-guided LVS debug environment

Assura Physical Verification offers a GUI debug environment that interactively steps users through the process of resolving LVS errors. Once the LVS run is complete, users can choose to open the LVS debug tools, such as the short locator and rewire function, from the pop-up window to examine and correct the errors.

Support of mixed-signal designs

Assura Physical Verification has the ability to recognize standard and special devices (e.g., n-terminal devices, drawn inductors, multi-emitter/collector bipolar
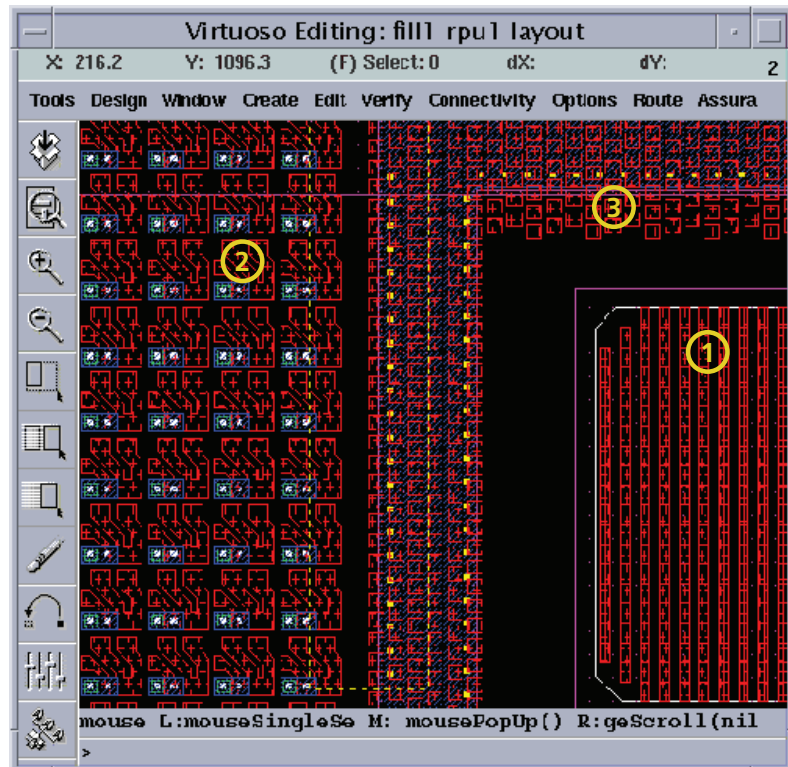

Figure 2. Sample context-dependent fill recipe: rectangular fill (1) under bond pad, grounded multi-layer custom fill (2) pattern in empty areas, skewed square fill (3) under power lines.
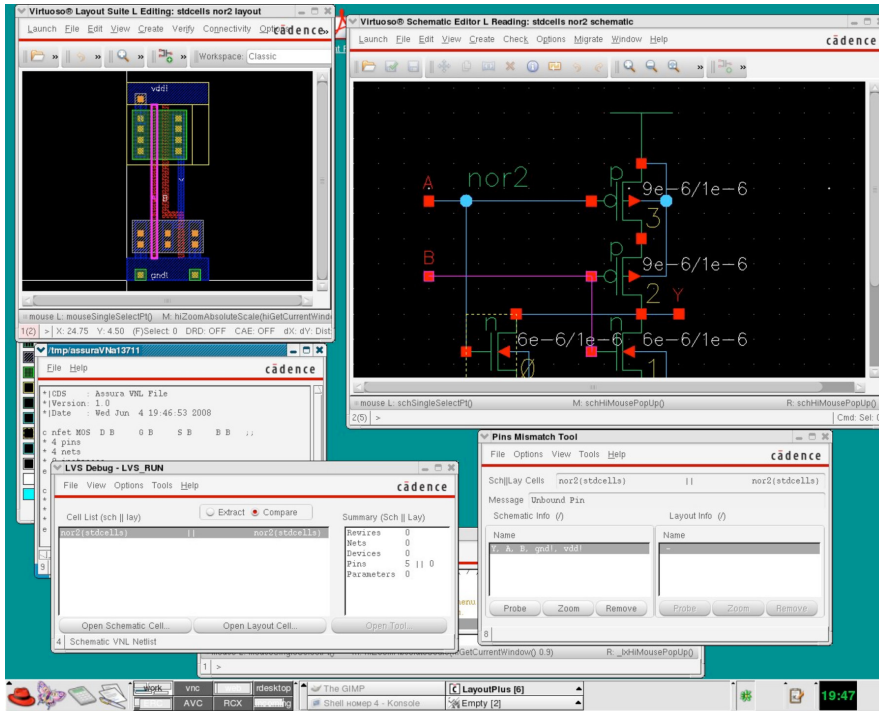
Figure 3. Assura Physical Verification offers a guided LVS debug environment, integrated into the Virtuoso Custom Design Platform, that accelerates rework and overall physical verification cycle time

transistors, STI, ROMs, etc.), making it an excellent choice for mixed-signal designs. All devices extracted by Assura Physical Verification are automatically netlisted and passed into Cadence QRC parasitic extraction to avoid double-counting during parasitic extraction. Assura Physical Verification also has the capability to process mixed-signal designs that combine schematics from CDL, SPICE, and Verilog.

Specifications

Powerful rule language/syntax

- Area-based rules allow multiple design rules on a single chip

- Pattern checking capability accelerates implementation of advanced checks

- Hierarchical area fill capabilities with support for customer-defined filler cells

- SKILL-based rules language facilitates complex data manipulations and DRC rules

- Comprehensive set of electrical rule checks

- Antenna rule syntax supports conjunctive, conditional rules and multiple checks in one run

- Advanced features include data snapping, end-of-line checks, corner commands

- Supports BSIM well proximity checks

- Width-dependent separation check (a.k.a. 90nm halation rule)

- Advanced via cluster checks

Easy-to-use graphical user interface (GUI)

- Tightly integrated with the Virtuoso platform

- Fast error correction using edit-in-place or descend modes within Virtuoso Layout Editor

- Access layout data in edit- or read-only modes

- Hierarchical error reporting and cross-probing for blocks, cells, devices, nets, and pins

- Show errors by rule type or by layout cell

- Immediate error and warning messages during interactive sessions via command interpreter window (CIW)

- Perform XOR comparison between two databases

- Support sign-off or false error marker exception handling

- Window DRC operation allows fast localized checking, especially useful during chip assembly or for last minute edits to reduce redundant checking and runtimes

- Time-to-error capability

- Integration with QuickView to open and debug large designs

- Ability to view interim layers (for rule deck developers)

Comprehensive GUI-guided LVS debugging tools

- Extraction errors

- Short Locator

- Open Locator

- Malformed Device Tool

- Comparison errors

- Nets Mismatch

- Devices Mismatch Tool

- Pins Mismatch Tool

- Parameters Mismatch Tool

- Rewire Tool

- Hypertext Netlist Form displays the schematic netlist that corresponds to your layout and allows hierarchical cross-probing for blocks, cells, devices, nets, and pins directly from the displayed schematic netlist

- Net and device probing for locating matched and unmatched nets and connected devices in the layout or schematic window

- Command interpreter window (CIW) logs user's actions for future use

Performance and capacity

- Patented hierarchical algorithms (cell repetition analysis, auto-adaptive partitioning and auto-array recognition) process large volumes of data

- Multiprocessor support for reduction in runtime (uses both rules-based and data-based parallelism to optimize runtimes automatically)

- Dynamic scaling (adaptive detection of available memory and cores)

- Restart function for interrupted jobs saves CPU time

- 32- and 64-bit platform support

- Remote job submission/LSF support

Virtuoso platform compatibility

- IC 6.x.x

- IC 5.1.41

Design inputs

- Cadence layout database / GDSII layout data (single or multiple GDSII files)

- SPICE/CDL netlists

- Verilog® netlists

- OASIS data

Design outputs

- Cadence layout database / GDSII

- Error markers

- Textual reports for debugging and archival purposes

- SPICE/CDL netlists

- Graphical error markers and textual reports for debugging purposes

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training

- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom

- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet

- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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