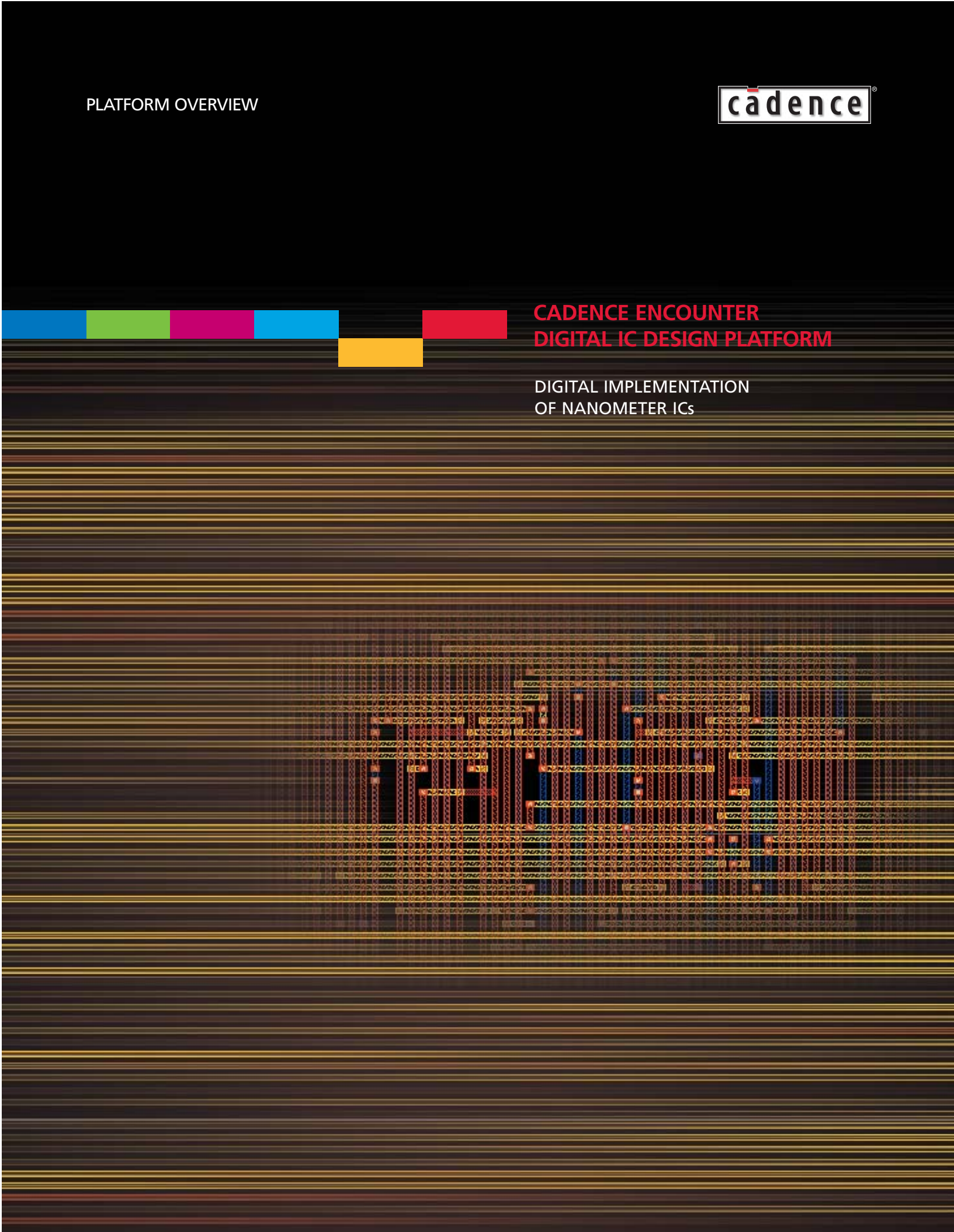
PLATFORM OVERVIEW

cadence®

CADENCE ENCOUNTER DIGITAL IC DESIGN PLATFORM

DIGITAL IMPLEMENTATION OF NANOMETER ICs



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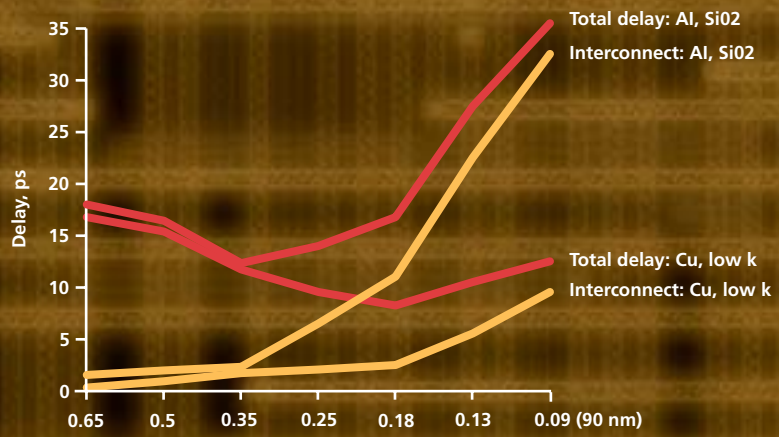
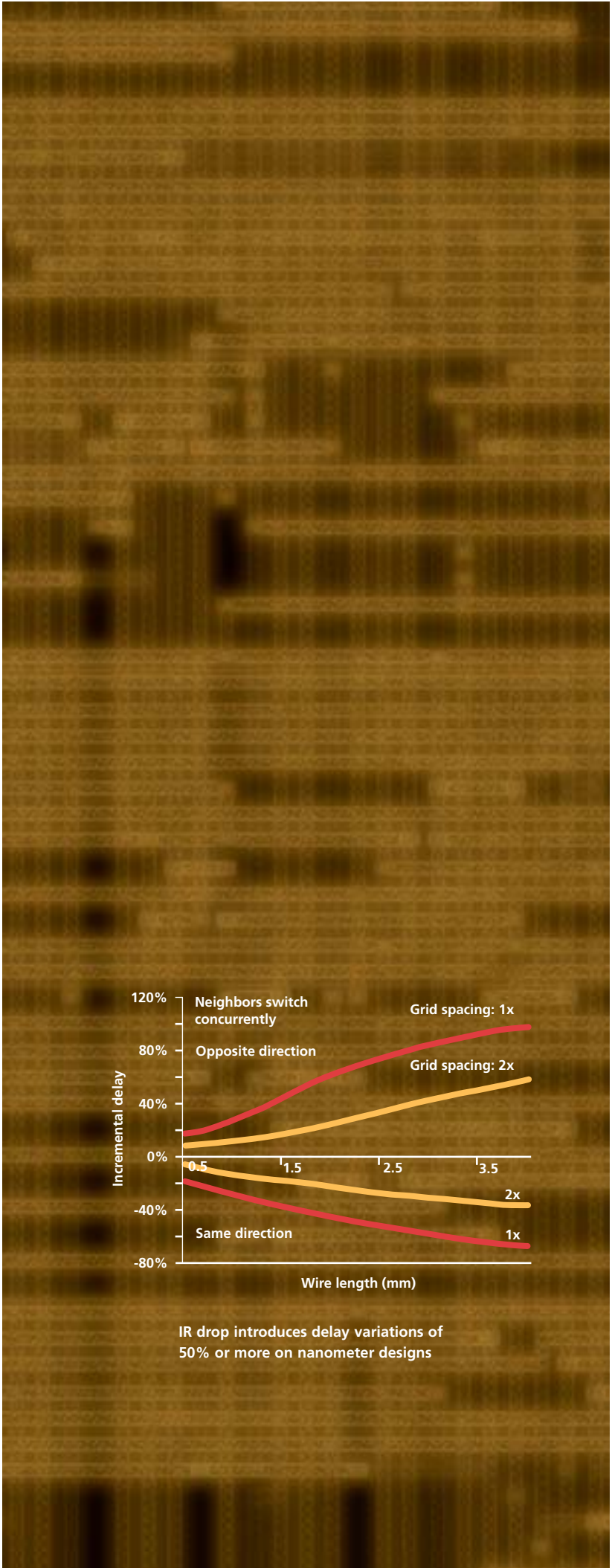


Wire delay exceeds gate delay at 0.18 micron and below in aluminum processes, and at 0.13 micron and below in copper



IR drop introduces delay variations of 50% or more on nanometer designs

THE FASTEST ROUTE TO LARGE, COMPLEX CHIPS

Before the advent of nanometer-scale process nodes, conventional design flows let you achieve fairly predictable results—and schedules. However, with chips growing increasingly larger and more complex, designers face an entirely new set of challenges. For instance, at 90 nanometers the percentage of total delay due to wire delay increases dramatically. Today's smaller geometries also exacerbate physical effects known to introduce significant problems—including signal integrity (SI) effects and IR (voltage) drop. The Cadence® Encounter™ digital IC design platform addresses these design challenges by delivering the best wires, minimizing full-chip iteration time, and maximizing quality of silicon (QoS)—a new measure of performance, area, and power that includes wires. It replaces traditional linear design flows with a completely new design strategy that incorporates the proven tools and methodologies for implementing extremely complex, high-performance chips.

CONTINUOUS CONVERGENCE

A MODEL OF PERFECTION

Since wire delay exceeds gate delay in today's large, complex chips, designers need a completely new methodology, one in which the effects of wires are known from the first day of implementation. The Encounter platform enables you to focus on "wires first" through the creation of extremely fast silicon virtual prototypes. These provide a detailed full-chip representation of a design — down to the routed wires. As chip development progresses, and more and more design decisions are finalized, the prototype is continuously refined to include the most complete and up-to-the-moment design information.

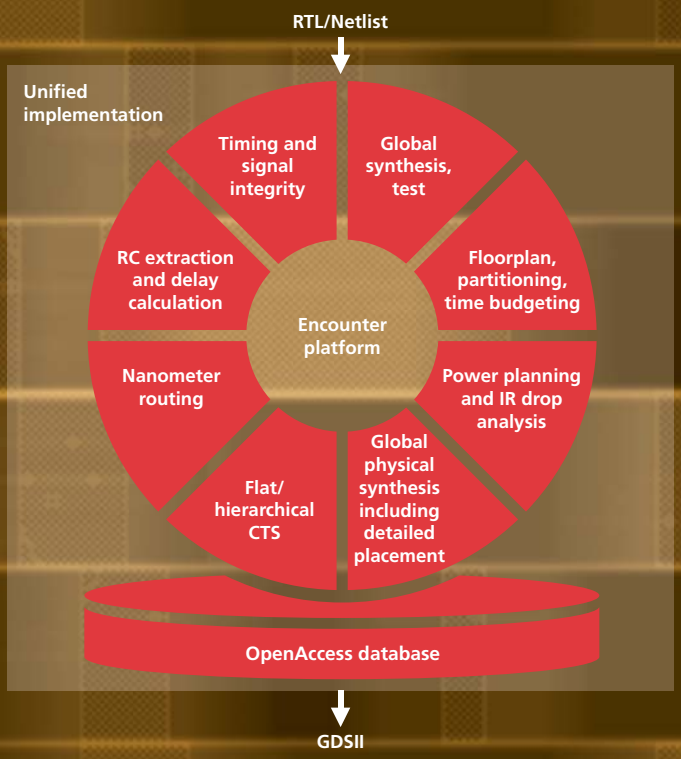
By using this "continuous convergence" approach, design teams know the exact status of their entire design on a virtually continuous basis, enabling them to always work on the most important issues. At any time, even on a daily basis, all design team members can check back on their work and respin the silicon virtual prototype. In this way, the team makes systematic, predictable, and measurable progress towards its performance and manufacturability goals. Once the team achieves all of its design specifications, the design can be taped out.

DELIVERING THE BEST WIRES

The Encounter platform leverages a unified architecture for full RTL-to-GDSII digital implementation for massive nanometer designs. It has the performance and capacity to deliver daily full-chip, full-wire iterations. Based on a single user interface and unified in-memory data model, it is specifically designed to focus on the core issue in nanometer digital implementation — delivering the best wires. Unlike traditional front-end/back-end systems, the Encounter platform does not require cumbersome and error-prone database translations between common tasks such as placement, clock tree synthesis, routing, and timing/crosstalk analysis.

ACHIEVING LOW POWER DESIGNS

Optimizing power is a critical goal in nanometer IC projects. The Encounter platform specifically addresses low power implementation challenges in nanometer designs by leveraging the proven convergence approach. It enables single-pass concurrent optimization of both leakage and dynamic power. Automatic level shifter insertion and placement further support multiple supply voltage design requirements. Other Encounter technologies enable you to accurately predict delays in chips that save power through the use of voltage islands (areas of cells operating at different supply voltages). You can also analyze the effect of voltage variations on noise and delay to ensure silicon-accurate performance in nanometer silicon.



The Encounter platform is a full-chip, single-architecture RTL-to-GDSII system

ENCOUNTER PLATFORM ARCHITECTURE

THE FASTEST ROUTE TO SILICON—HIERARCHICAL OR FLAT

The Encounter platform architecture serves as the foundation for a suite of specific product configurations:

- The Cadence SoC Encounter™ Global Physical Synthesis (GPS) system addresses hierarchical designs, with full-chip RTL-to-GDSII support for 50M+ gate chips
- The Cadence Nano Encounter™ configuration supports gates-to-GDSII implementation for flat chips and blocks of up to 5-10M gates on 32-bit machines

Encounter digital IC design platform products and capabilities include:

- RTL synthesis (Encounter RTL Compiler)
- Silicon virtual prototyping including global physical synthesis (Cadence First Encounter® Global Physical Synthesis [GPS])
- Nanometer routing (Cadence NanoRoute™)
- Signal integrity and analysis with delay calculation (Cadence CeltIC™ NDC)
- Signoff extraction (Cadence Fire & Ice® QXC)
- Power grid analysis (VoltageStorm)
- Equivalence checking (Encounter Conformal®)
- Test solution (Encounter Test)

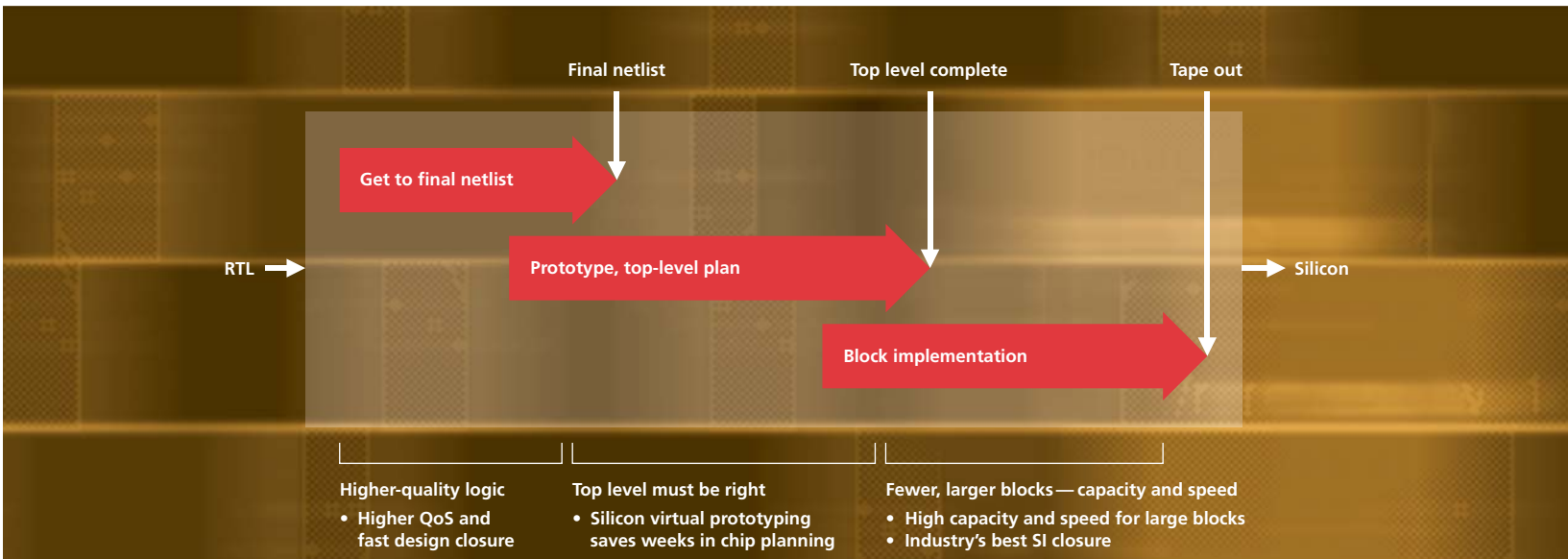
GLOBAL SYNTHESIS FOR SMALLER, FASTER, LOWER POWER DESIGNS IN LESS TIME

Cadence Encounter RTL Compiler lets you accurately circumnavigate the RTL synthesis implementation space and simultaneously consider timing, area, and leakage and dynamic power in a single optimization pass. It incorporates new global optimization algorithms that enable multi-objective optimization. Proven as a critical element in timing closure for 90nm and 65nm designs, this technology helps engineers tackle many types of advanced digital IC designs in which power has become a key consideration.

INDUSTRY-STANDARD SILICON VIRTUAL PROTOTYPING INCLUDING GLOBAL PHYSICAL SYNTHESIS

In addition to serving as a universal cockpit for the Encounter platform, Cadence First Encounter® GPS is the industry's premier silicon virtual prototyping system. Unlike traditional physical synthesis solutions that optimize a single logic path at a time, it optimizes timing closure for many paths concurrently. This global physical synthesis capability allows First Encounter GPS to reach timing closure on large blocks faster—cutting the time required from days to hours in many cases.

Designers use First Encounter GPS to drive all tools and functions, combining all aspects of implementation and analysis within a single, full-chip environment. These functions include: floorplanning, partitioning, hierarchy management, logic synthesis, physical synthesis, placement, trial routing, final detailed routing, clock tree synthesis, power planning, power grid analysis, timing analysis, and signal integrity analysis. Design teams use this consistent view of their design throughout the continuous convergence methodology.



Shorten your design cycle with the Encounter platform

TRUE NANOMETER ROUTING

Cadence NanoRoute™ is an independent routing, optimization, verification, and chip-finishing solution that operates natively within the Cadence SoC Encounter GPS system and seamlessly with other industry design flows. With its patent-pending concurrent S.M.A.R.T. routing (unified signal integrity, manufacturing aware, routability, and timing optimization) and superthreading technologies, NanoRoute takes an already placed gate netlist and generates a tapeout-ready GDSII design database that meets the timing, signal integrity, process rule, and manufacturability requirements of nanometer design—in a fraction of the time other routing solutions take.

INTEGRATED TIMING AND SIGNAL INTEGRITY CLOSURE

The Encounter platform features integrated optimization using global synthesis technology for rapid timing and signal integrity closure of complex nanometer designs. This enables the industry's fastest runtime and accommodates designs of over one million placeable instances on 32-bit machines. Within the Encounter platform, timing and signal integrity are optimized at every stage, including prototyping and placement—both during and after routing.

To achieve signal integrity closure, crosstalk delay, and glitch effects are considered using an embedded version of the CeltIC Nanometer Delay Calculator (NDC)—widely recognized by leading silicon vendors for precision signal integrity sign-off.

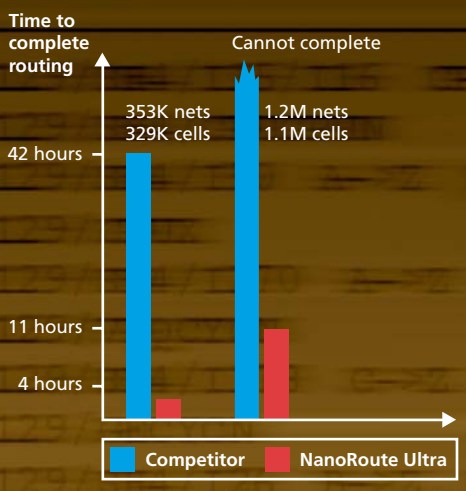
Celtic NDC combines the capabilities of the previous version of Celtic with SignalStorm Nanometer Delay Calculator (NDC). Encounter leverages CeltIC's ability to significantly reduce false violations, which speeds SI closure by avoiding unnecessary repairs.

Encounter also utilizes effective current source modeling (ECSM) for accurate prediction of nanometer delays, including voltage variation caused by supply voltage (IR) drop or voltage scaling. The result is a highly efficient and tightly integrated approach to timing and signal integrity closure.

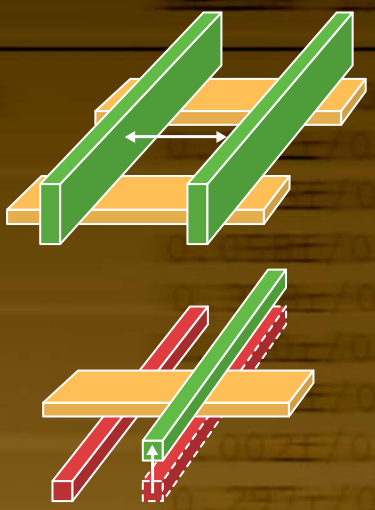
In addition, the combination of Cadence Fire & Ice QXC 3D-accurate parasitic extraction, the Cadence VoltageStorm® power grid verification product family and Cadence CeltIC NDC enables highly accurate signal and power integrity-aware timing sign-off flows, including support for third-party tools using industry-standard file formats.

ACCURATE PARASITIC EXTRACTOR

Cadence Fire & Ice QXC combines 3D-accurate parasitic extraction with bounded coupling capacitance accuracy to enable the most accurate timing, power, and signal integrity sign-off flows. It is tightly integrated with crucial analysis products like the Cadence VoltageStorm product family and the Cadence nanometer timing solution. It also supports third-party tools through industry standard file formats.



NanoRoute graph-based technology delivers the routing capacity and performance required for nanometer-scale SoC designs



Timing and crosstalk are automatically calculated during routing and used to make on-the-fly decisions such as layer assignment and wire spacing

EQUIVALENCE CHECKING AND CONSTRAINT DESIGN

The Encounter Conformal Equivalence Checker (EC) offers you the only complete equivalence checking solution available for verifying complex SoC designs from RTL to layout. It verifies the widest variety of circuits, including complex arithmetic logic, datapath, memories, and custom logic. Encounter Conformal EC also provides the highest performance and completion rate in verifying circuits that other formal tools leave unchecked.

Encounter Conformal Constraint Designer automates the validation and modification of constraints and ensures that timing constraints are valid throughout the entire design process. Based on the proven formal engine, it checks design constraints for correctness, validates exceptions functionally, checks hierarchical constraint consistency, and generates timing exceptions. By pinpointing real design issues quickly and accurately, Encounter Conformal Constraint Designer helps designers achieve rapid timing closure.

SOC POWER INTEGRITY VERIFICATION

Also included in the Encounter platform is the leading power grid verification solution and first transistor-accurate power grid analysis product—Cadence VoltageStorm power integrity verification. It applies production-proven IR drop analysis early to prevent costly downstream ECOs for correcting power grid problems. Using VoltageStorm to verify power grids before and after signal routing helps eliminate overdesign, increases flexibility for signal routing, and eases the timing closure burden. In addition, VoltageStorm enables a static timing analysis (STA) flow by feeding instance-based operating voltages into the Cadence nanometer timing solution. The STA flow includes both SI analysis and IR drop analysis to avoid timing failure and failed silicon.

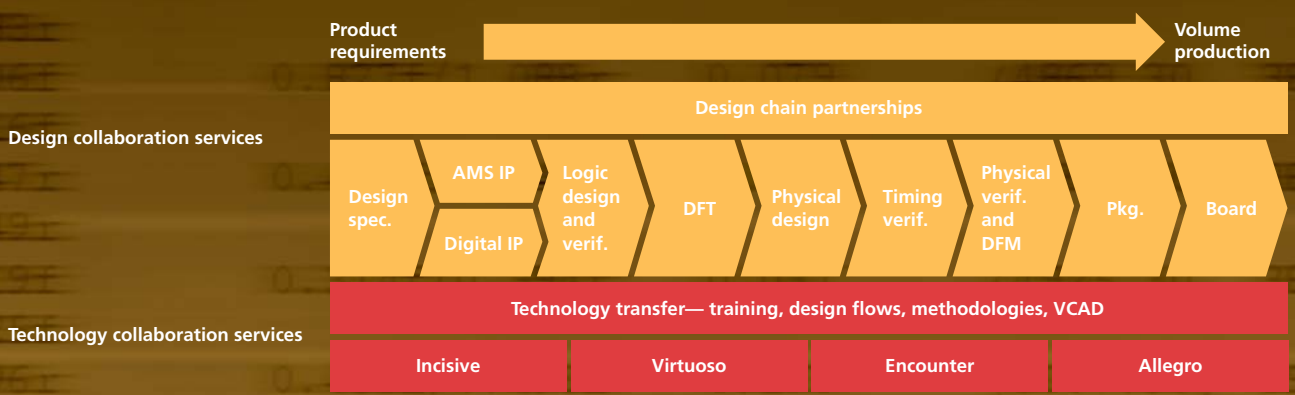
NANOMETER TEST

Based on over 25 years of technical innovation and proven on over 10,000 ICs—spanning the entire range of design styles—Cadence Encounter™ Test delivers the industry's most advanced comprehensive test solution. Full-chip DFT insertion and verification delivers fast time to market; low-impact OPMISR+ compression minimizes the cost of test; True-Time delay test provides unparalleled product quality; and yield diagnostics delivers rapid ramp to yield.

For more information about nanometer design, the Cadence Encounter platform, and associated services, visit **www.cadence.com/encounter**.

PARTNERING FOR SILICON SUCCESS

Cadence Engineering Services supports your product development team to ensure the lowest risk path to product success. Choose from the industry's broadest array of proven design tools and methodologies. You can also leverage our world-class design expertise and technology partnerships with key industry leaders.



Cadence Design Systems, Inc.

Corporate Headquarters
555 Seely Avenue
San Jose, CA 95134
800.746.6223
408.943.1234
www.cadence.com

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