Using Cadence Chip Optmizer with SOC Encounter GXL for Design Closure

By

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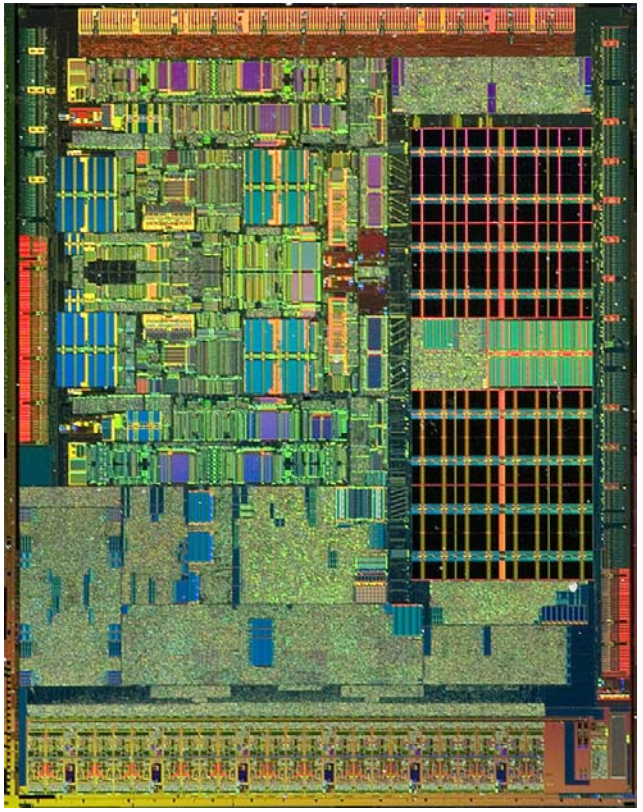
Outline of the Presentation

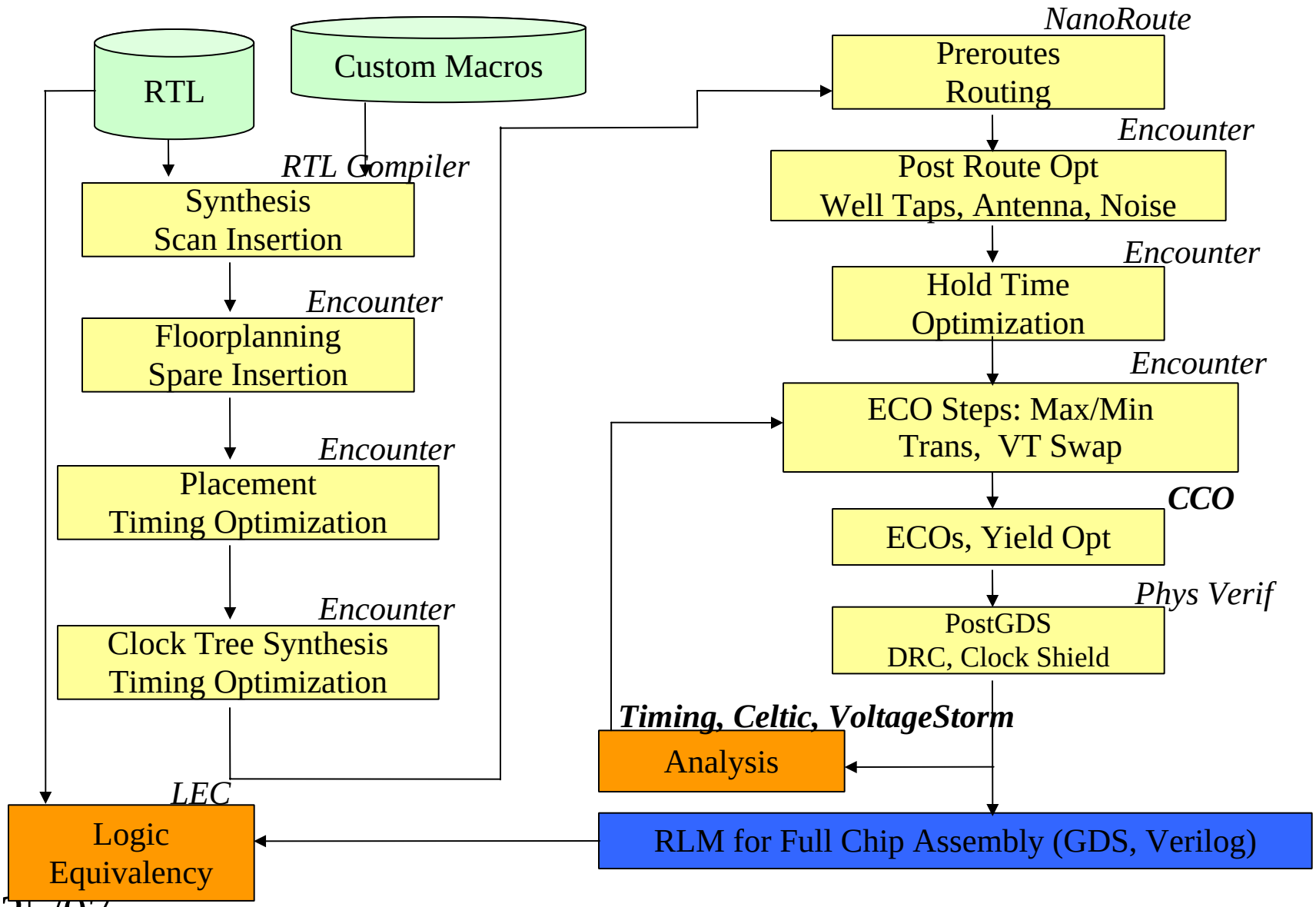
- Background of the Design
- Cadence Chip Optimizer (CCO) Flow Integration
- ECO Experiments
- Yield Improvements
- Technology Rule implementation
- Summary and Future Work

Background

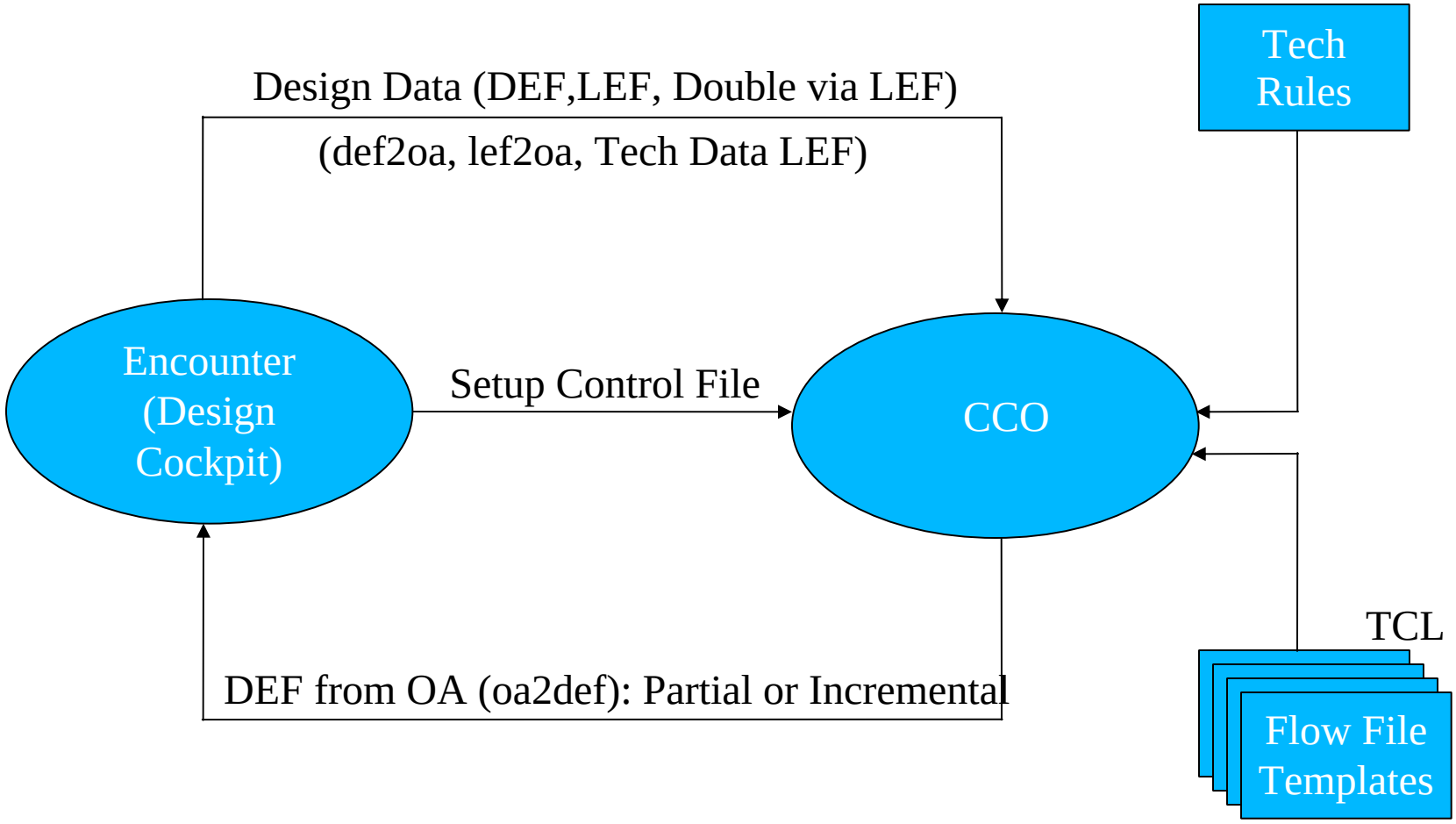
- SoC Design
- Semi-Custom Methodology
- PowerPC CPU running @ 2GHz
- 65nm Technology
- 40% running at 2GHz and 40% at 1.1GHz
- Cadence Implementation Tools
  - SOC Encounter



SOC Physical Synthesis Flow



CCO Integration in Flow

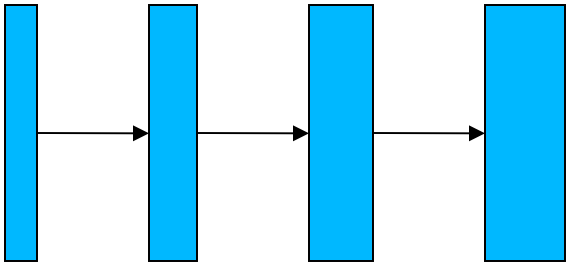


ECO Experiments

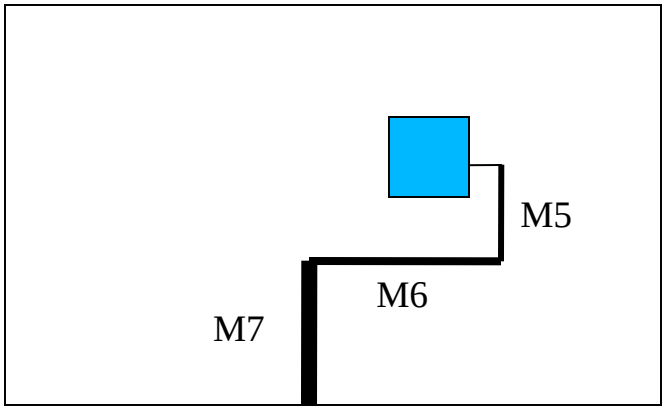
- Wire Widening
- Shorts and DRC Fixing
- Technology File Add-Ons
- Yield Optimization
  - Via Reduction
  - Jog Removal
  - Via Doubling

Wire Widening

- Timing Improvements
- Reduce Resistance of wires
- Taper Wires
- M5-M7 for maximum benefits on long wires
- 3 Steps of changes to Widths of wires
- Output versus input Long wires
- Noise Flow Robust



wire width increased in 3 steps



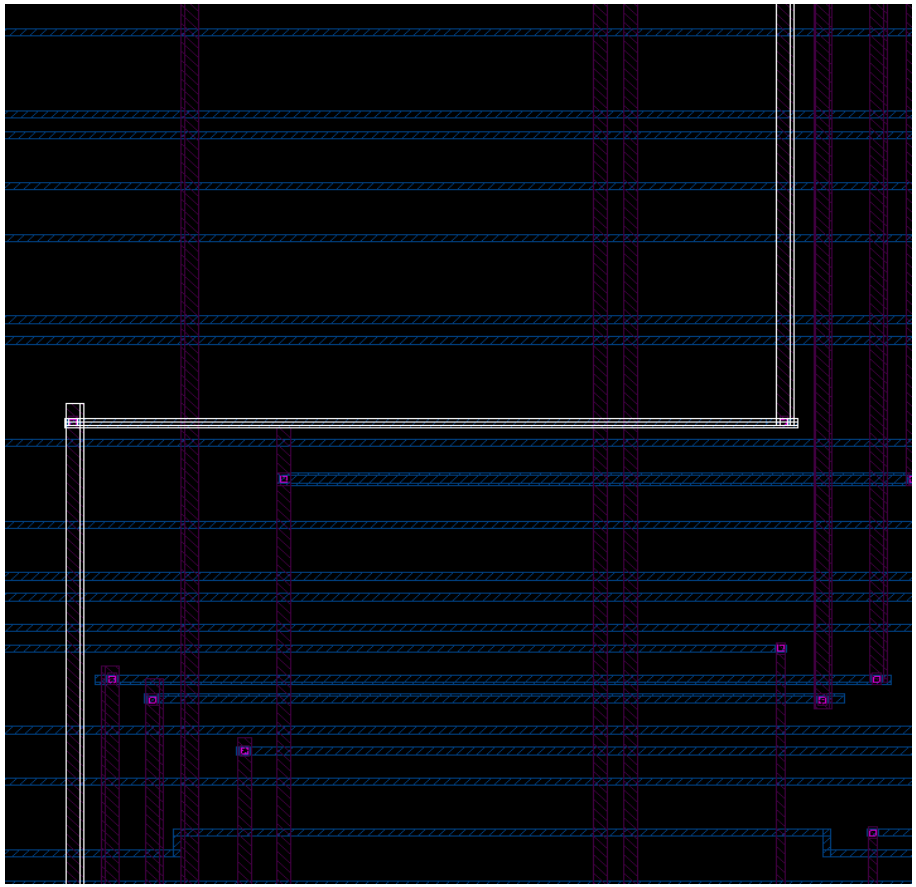
Tapering from input pin

Wire Widening Results

- Timing improvements on a critical bus (descending order)

Net	Before	After wire widening	Difference
	Delay(ps)	Delay(ps)	(ps)
Net[13]	27.95	20.9	**7.05**
Net[18]	22.51	15.88	**6.63**
Net[0]	27.51	21.39	**6.12**
Net[3]	25.45	19.82	**5.63**
Net[38]	14.69	10.48	**4.21**
Net[45]	13.22	9.16	**4.06**
Net[46]	11.45	7.4	**4.05**
Net[49]	12.86	9.44	**3.42**
Net[24]	25.5	22.45	**3.05**
Net[54]	11.11	8.16	**2.95**
Net[42]	13.98	11.2	2.78
Net[41]	15.62	13.97	1.65
Net[62]	10.49	9.01	1.48
Net[36]	18.21	17	1.21
Net[33]	25.79	24.59	1.2
Net[37]	16.26	15.29	0.97
Net[48]	14.42	13.65	0.77
Net[44]	12.83	12.28	0.55
Net[14]	22.99	22.85	0.14

- Snapshot of a net that is widened



Shorts and DRC Reduction

- Encounter not clean on 65nm Design Rules
- Complex Rules
- Congested blocks
- Grided versus Gridless fixing
- Option CCO: set_route_on_grid
- ECOs in Encounter, a consideration

Technology Add-On

- 65nm rules
- TCL Interface for custom design rules
- Minimum Enclosure rules
- End-of-Line rule
- Minimum Area rules, based on number of Vias present on the wire above and below
- Protrusion proximity spacing rule

Examples of Design Rule Coding

- Minimum via enclosure rule for via1 in metal1 and metal2 (values are in microns)
  - *set_layerpair_constraint -constraint minDualExtension -DualDBUValue { 0.005 0.040 } -layer1 MET1 -layer2 VIA1*
  - *set_layerpair_constraint -constraint minDualExtension -DualDBUValue { 0.005 0.035 } -layer1 MET2 -layer2 VIA1*
- *Check space as max of x or y (cannot use diagonal distance between metal)*
  - *set_layer_constraint -constraint checkSpaceAsMaxXY -BoolValue true -hardness hard -layer MET1*
- minSpace rules on samenet. Specified as one dimensional table with first 2 values for width range and the next value for spacing.
  - *set_layer_constraint -group foundry -layer MET1 -constraint minSameNetSpacing -hardness hard -row_name width -OneDTblValue { 0 0.1 0.11 0.1 0.185 0.13 0.345 0.15 0.595 0.18 1.125 0.23 2.165 0.47 } -row_interpolation snap_down -row_extrapolation {snap_up snap_down}*

Shorts and DRC Reduction Results

- Design Statistics for 2 blocks considered

	Cells	Nets	I/Os	Area (sq microns)	# std cells	# special	# macros
Block E	142617	151757	2067	2266400	141169	1444	4
Block F	500082	534647	3403	5765162	498636	1433	13

- Block E had opens that had to be manually routed
- Block F is a large ASIC block with half million gates
  - DRC reduction without CCO would have taken one man week

	Before				After CCO			Runtime
	Opens	DRCs	Shorts		Opens	DRCs	Shorts	
Block E	105	250	0		0	15	0	1hr
Block F	0	1614	0		0	150	0	4hrs

Yield Optimization

- Optimization of Design for maximum implementation of recommended rules
  - Via Reduction
  - Jog Removal
  - Via Doubling
  - Shorts and DRC Reduction
  - Post CCO verification

Via Reduction

- Design Statistics for 3 blocks considered - A, B & C

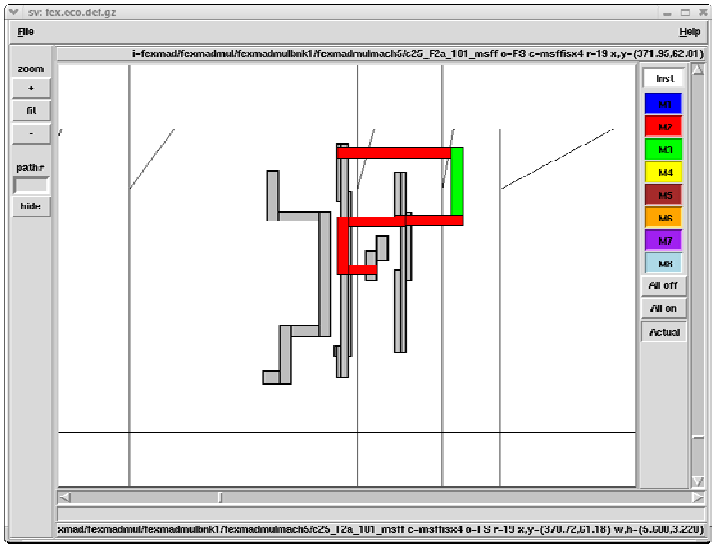
	Cells	Nets	I/Os	Area (sq microns)	# std cells	# special	# macros
A	8699	10357	935	1395670	8617	80	2
B	47671	55833	657	1055088	47143	526	2
C	148303	163798	1929	1871289	148265	0	38

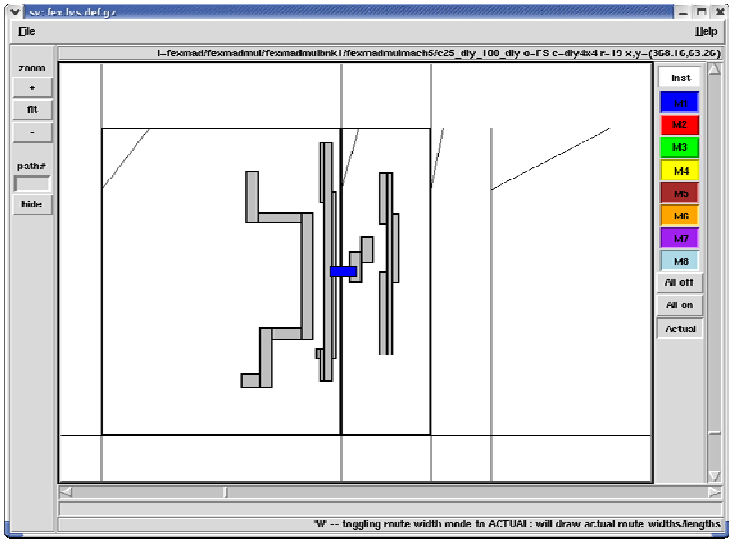
- Via reduction on the 3 blocks A, B & C
  - On an average 14.5% reduction in vias

	A			B			C		
Layer	Before	After	% reduce	Before	After	% reduce	Before	After	% reduce
Via1	26586	25871	2.69	162549	153645	5.48	551435	511125	7.31
Via2	20234	17757	12.24	164910	137921	16.37	537667	441375	17.91
Via3	6664	3916	41.24	69581	47481	31.76	247926	163545	34.03
Via4	4434	3454	22.1	39819	32636	18.04	100921	75928	24.76
Via5	2681	2482	7.42	6312	5605	11.2	28373	24088	15.1
Via6	1907	1554	18.51	4946	2885	41.67	17101	14091	17.6
Total	**62506**	**55034**	**11.95**	**448117**	**380173**	**15.16**	**1483423**	**1230152**	**17.07**

Jog Removal

- Before and After CCO snapshot of routes of one net
  - Lot of local routes are routed in horizontal M1 saving vias and M2 tracks





Via Doubling

- On an average 55% Via doubling
- Block A and B are custom blocks while block C is ASIC
- In general good %age of double vias inserted

	A			B			C		
	# before	# after	% of total	# before	# after	% of total	# before	# after	% of total
Via1	0	12692	49.06%	0	71853	46.77%	0	208657	40.82%
Via2	37	12958	72.97%	223	105966	76.83%	0	297712	67.45%
Via3	53	2842	72.57%	340	29518	62.17%	0	76043	46.50%
Via4	24	2860	82.80%	179	22960	70.35%	0	44857	59.08%
Via5	0	700	28.20%	0	2679	47.80%	0	12605	52.33%
Via6	0	1025	65.96%	0	2352	81.53%	0	8572	60.83%
Total	**114**	**33077**	**60.1**	**742**	**235328**	**61.9**	**0**	**648446**	**52.71%**

Summary

- CCO Integration with Encounter
- ECO's in CCO
- Yield Optimization
- Timing Improvements
- Technology Rule Implementations

Future Work

- Complex DRC Rules
- Wire Spreading on Critical Nets
- Structured Routing/CSR
- Flow Integration

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