An Effective EM/IR-drop Flow with UltraSim and VAVO/VAEO

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ABSTRACT

Both static and dynamic methods are widely used for the electro-migration (EM) and IR-drop verifications. For analog and mixed-signal (AMS) designs, only dynamic spice-like simulations may provide adequate accuracy. It is well-known that dynamic simulations generally take a long run time even with so-called fast spice simulators, such as UltraSim. In addition, the EM and IR drop verifications require the power/ground (P/G) parasitics extracted, which will slow down the simulation many times. Furthermore, some AMS designs, such as analog-to-digital converters (ADC), need a long transient simulation time to settle down. Until then, the EM and IR drop measurements cannot be started. To overcome the runtime problem, an effective EM/IR-drop flow has been developed at National. This flow takes advantage of some UltraSim's new features, such as EMIR, and shorting the P/G nets, etc. and has achieved huge speed-up for the EM/IR-drop simulations without any accuracy compromise.
The essential of the flow is a two-phase approach. In phase one, all the P/G nets are shorted, and a simulation status is saved in the end at which the AMS circuitry has settled down. In phase two, all the RC parasitics is kept as is, the saved status is reloaded, and the usim_emir option is turned on with start parameter equal to the time at which the status was saved.
In general, the transient simulation time is much longer in phase one than in phase two. Because of the shorted P/G networks in phase one, the run time may be shortened several or even more than ten times compared to that in the corresponding non-shorted P/G simulations. With the short transient simulation time and the EMIR option, VAVO/VAEO is able to process the emir results much faster and to achieve much better accuracy for both EM and IR-drop analyses.
The paper will describe our EM/IR-drop flow in detail, and share our experiences and lessons with the Cadence user community. The case study on two real designs will show the efficiency and effectiveness of this flow.
Because this flow is almost solely based on Cadence ASSURA, UltraSim and VAVO/VAEO, it should be easy for other Cadence users to adopt it.

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1.0 Introduction

Both electro-migration and voltage drop are important physical verifications, especially for designs using nanometer technologies. In such advanced technologies, power voltages become close to the transistor threshold voltages, which makes transistor performance more sensitive to the P/G voltage changes. Furthermore, interconnect routings become very narrow, resulting in an increasing sensitivity to electro-migration effects.

It is well known that the electro-migration verification requires average, peak and/or RMS current density information. If the current in the metal flows in one direction, failures are mainly caused by material transportations, and the average current should be used for EM checks. On the other hand, if the current flows bi-directionally, thermal effect will be the main cause for failures, and the RMS current should be used.

As for voltage drops on the P/G grids, conventionally so-called IR-drop, the average drop i.e. DC drop may reveal connection defects, such as missing or too few vias/contacts, too narrow routing metal widths, etc. But only DC drop checks are not enough. The dynamic voltage drops must be checked to guarantee the performance of the circuit, either digital or analog, to meet the design specifications.

In a digital circuit, the average/RMS/peak current values and P/G grid voltage drops may be calculated by gate-level static simulations. For example, the average/RMS current of a gate can be calculated with the switching rate and slew information available from functional and timing simulations previously done. By the special characterization of library gates, dynamic IR-drop analysis may also be done statically. This kind of static analysis can handle very large designs with millions of gates, and is much faster than Spice-like dynamic simulations.

Unfortunately, because of the analog characteristics, similar static methods cannot be applied to analog circuits in order to obtain average /RMS current and voltage drop values within an acceptable range of accuracy. For analog or AMS designs with dominant analog part, i.e. so-called big A small D designs, direct Spice-like simulations become the preferred choice to obtain the current and voltage drop information required for the EM and IR-drop verifications.

For the EM verification purpose, all interconnect metals need to be checked. Therefore a detailed interconnect parasitic resistance extraction must be performed. Because of the special requirements for the EM verification, parasitic reduction is seriously limited, resulting in a huge parasitic netlist with hundreds of thousands, even millions of parasitic resistors.

Because of very large amount of parasitic resistors in the power and ground nets, a Spice-like simulation becomes very time consuming. In addition, the average/RMS current flowing through each resistor must be measured in order to check if there is any EM violation for the corresponding piece of metal or via. This measurement process typically takes even longer time than the simulation itself, and has become the bottle neck of the whole EM verification flow.

For an IR-drop analysis, the situation may be slightly better. Because the interested nodes for voltage drop checks are only the device P/G terminals, more aggressive RC reductions may be

carried out. But for the purpose of dynamic IR-drop analysis, both R and C of the power grids must be extracted since parasitic capacitors are capable of smoothing voltage variations, thus reducing the dynamic voltage drop.

By using some special options of UltraSim, especially .usim_emir and .usim_pn options in the input deck, the EM/IR-drop verifications may be dramatically simplified and the accuracy may be significantly increased. In addition, VAVO/VAEO processing time may also be reduced because calculations of average/RMS/peak current and voltage drop have already been done by UltraSim during the transient simulation.

This EM verification flow for large analog and AMS designs has been applied to several large AMS designs at National, and has been proved to be very effective. The settings related to the UltraSim input deck will be described in the following sections of the paper. The whole EM/IR-drop flow and its effectiveness and limitations will also be discussed in detail.

Since the EM verification for power and ground nets is much more challenging than that of signal nets, the paper will be focused on power and ground nets.

2.0 Parasitic Extraction with Assura RCX

In order to save runtime, different Assura RCX extraction setups and options should be used for different verification purposes. Typically, the runtime of Assura RCX extraction is much shorter than the runtime of UltraSim simulations. Therefore it is not a good idea to use one most complete parasitic netlist with everything for all purposes, except for very small designs.

For the P/G EM verification purpose, the P/G-only extraction may be used. For the signal nets EM verification, all the P/G nets may be excluded. For the IR-drop check, full P/G RC should be extracted with aggressive RC reductions. With these different parasitic netlists, the simulation time can be dramatically reduced with an insignificant loss of accuracy.

All the physical verifications and parasitic extractions are based on the design layout. The layout is a two-dimensional view, say X-Y dimensions. The other dimension of the design, say the vertical or Z dimension, is solely determined by the chip manufacturing process. The parameters of the vertical geometry, such as the metal thickness of a specific metal layer, the via height of a specific via layer, etc., are the same for all the designs using the same manufacturing process. Therefore, current densities in the EM specification for metal layers are typically expressed in current per unit width, not in current per unit area. For a specific manufacturing process, different metal layers may have different values of thickness. More importantly, the interconnect metal pieces of different metal layers are connected through so-called vias. Because metal layers and vias have different EM specifications to comply with, resistors belonging to different metal or via layers in the extracted parasitic netlist must not be merged. In addition, resistors of different widths cannot be merged either, even if they belong to the same metal layer.

To implement the ideas mentioned above, the selection of specific Assura RCX options will be discussed in the following sub-sections.

2.1 Selections in the Extraction Tab

As explained before, except for the very small designs, Full Chip All Nets should not be used. For P/G EM or IR-drop verifications, Full Chip Selected Nets may be selected, and for signal nets EM verifications, Excluded Nets may be a better choice. Typically there are only a small number of power nets, and a much bigger number of signal nets. It is more convenient to list a small number of nets, either by direct listing or through a file.

For P/G EM checks, the R-only extraction may be enough. But for signal nets, full RC should be selected. This is because the RMS current values are heavily dependent on the variations of wave forms. Without capacitance, the RMS current values could be significantly bigger than they really are.

For IR-drop checks, full RC extraction must be selected to avoid unreal spikes in the voltage wave forms.

2.2 Selections in the Filtering Options Tab

In this form, dangling resistors should be removed by selecting Dangling R. In addition, MinR may be raised a bit from 0.001 Ohm to 0.01 Ohm, which may reduce the number of parasitic resistors significantly. According to our experience, it is necessary to merge vias/contacts except for very small designs. Otherwise the generated parasitic netlist will be too big to handle. So it may be a good choice to keep the default value auto for Max Merged Via Size and Array Vias Spacing.

As mentioned previously, if the extraction is for IR-drop checks, Reduce RC should be selected, and a low frequency number may be entered for RC Frequency (MHz) for a more aggressive RC reduction.

2.3 Selections in the Netlisting Options Tab

According to the Assura user guide [1], selecting Add Explicit Vias in the RCX Netlisting Options Tab can avoid the merge of via/contact resistors and parasitic metal resistors. Therefore this option should be selected for the EM check purpose. In this tab, Parasitic Resistance Width should be selected because the width parameter is necessary for current density calculations. Parasitic Resistance Length should also be selected to avoid netlisting multi-width parasitic resistors, according to the Cadence application engineers. But it was found that Assura RCX sometimes still failed to separate metal pieces with different widths, even if this option was selected.

Fig. 1 is a working example of the Assura RCX run reference file (RSF) for P/G EM verifications. Only the relevant part has been shown. The options expressed in bold letters are those discussed previously, except for ignoreVias, which will be discussed in the following.

```
...
rcxParameters(
        ?outputFormat   "dfII"
        ?extractedView  "av_R"
        ?checkCellView  nil
        ?resistor       "presistor"
        ?resPropName    "r"
        ?extract    "res"
        ?netNameSpace   "layout"
        ?rcxfsType  "none"
        ...
        ?danglingR     t
        ?minR  0.01
        ?maxMergedViaSize  "auto"
        ?arrayViasSpacing  "auto"
        ...
        ?parasiticResWidth  t
        ?parasiticResLength  t
        ?xyCoordinates  ( "r" )
        ?ignoreVias ( layers("psubstrate_pdifp_connect"
"nwell_ndifn_connect" "high_nwell_connect" "high_sub_connect")
nets("pwrp" "pwrn") )
        ?substrateStampingOff  t
        ?addExplicitVias  t
        ?runName  "sha250"
)
avRCX()
```

Fig. I An example of Assura RCX Run Reference File

Assura RCX has a problem to deal with the well-tie extractions. If the option ignoreVias is not selected, the resultant P/G parasitic nets may include a lot of very small resistors (0.01 Ohm), connecting all the N or P well ties, respectively. This may partially short the P/G nets, and result in wrong current values of P/G parasitic resistors from the simulation. By ignoring the well-ties in the P/G nets during netlisting, transistors' bulk terminals will be connected directly to the power or ground pins, respectively.

3.0 EM/IR-drop verification simulations with UltraSim

3.1 Setting UltraSim options

To check the current density on each piece of the interconnect metal and vias, it is highly desired to use the extracted parasitic netlist as the input netlist directly to obtain the average/RMS/peak currents on each parasitic resistor of the power and ground nets, or to obtain the voltage drop at each transistor terminal connecting to the power or ground grid.

UltraSim is a so-called fast Spice simulator, and provides a rich set of accuracy-speed tradeoff parameters. In all the accuracy-speed tradeoff parameters, SIM_MODE and SPEED [2] are two of the most critical performance control parameters for the EM and IR-drop simulation of large

AMS designs. The SIM_MODE parameter controls the device modeling and simulation partitions, and the SPEED parameter controls the error tolerance of iterations. For some AMS designs, such as analog to digital converters (ADC), The sim_mode a (analog) should be used. Otherwise the simulation may fail because of the convergence problem.

Traditionally, UltraSim generates voltage waveforms for all the interested nodes. Then VAVO/VAVEO processes the saved voltage waveform data, and calculates average/RMS/peak currents or voltage drops. The current value is calculated using the voltage difference of two terminals of a parasitic resistor divided by its resistance. In many cases, both the voltage difference and resistance value are very small, resulting in a significant accuracy loss. To avoid this, the double precision may be used to store the waveform data, and the SPEED may be set to a small number, such as 2 or 3. But either of them has a significant negative effect. First, using double precision to store the waveform data roughly doubles the size of the waveform data file. Typically, the waveform data file is already very big with default single precision setting. Doubling the size makes it even more difficult to process, resulting in much longer runtime for VAVO/VAVEO. Secondly, it takes much longer time for UltraSim to finish the simulation with a reduced SPEED number.

Recently, UltraSim introduced a new option called .usim_emir (It is available for UltraSim version 6.1 or newer). With this option turned on, UltraSim will generate a data file with all the average, RMS and peak values of voltage on each node and current on each resistor. If the emir data format is set to *[VAVO]*, the file will have an extension *.emir0_vavo.db*. VAVO/VAVEO can read in this binary file and generate EM and IR-drop violation reports.

Since the average/RMS/peak values are directly available in the emir data file and no further calculation is required, VAVO/VAVEO is able to generate the reports much faster than before. In addition, since the average/RMS/peak values are calculated in double precision during the transient simulation, the accuracy of the results is much better than that achieved by the traditional VAVO/VAVEO flow if the same option parameters are used.

3.2 How to resolve long settle-down runtime problem

The runtime and data size are highly dependent on the number of parasitic elements, such as parasitic resistors and capacitors, especially when these resistors and capacitors belong to power/ground nets. For P/G EM checks, parasitic reduction is severely limited, resulting in the P/G networks with hundreds of thousands, even millions of parasitic elements. In addition, it takes long time for some AMS circuits, such as an ADC, to achieve the working status, and the meaningful current measurements cannot be started until the stable status is reached.

To resolve the runtime problem, it is better for the initial simulation to generate only a status dump at a time after the circuit has settled down. The simulation for the emir data generation will start from that time by reloading the status dump saved before. With exactly the same parasitic netlist, an aggressive power/ground parasitic reduction becomes possible for the first simulation since no emir data is generated. In the second simulation, the time interval for the average/RMS/peak currents and voltages can be set as short as possible to save the runtime further. The .usim_emir option allows a user to specify the start time and stop time for emir data

generation. If the time interval for the emir data is different from that of the transient simulation, this feature provides a user with the desired flexibility. Section 3.3 discusses more details about UltraSim options setting.

3.3 An example of UltraSim options setting

```
…
tran tran stop=900e-9
simulator lang=spice lookup=spectre
...
.usim_opt sim_mode=a wf_format=SST2
.usim_opt postl=0
.usim_restart FILE=save800N.usim_25C@8.000000e-07
.usim_emir format=[VAVO] start=801n stop=900n
```

Fig. 2 An example of UltraSim options setting

Fig. 2 shows an example of UltraSim options setting. This is an ADC design, therefore analog simulation mode is used (sim_mode=a). The option postl=0 is chosen for final emir data generation since no parasitic reduction is allowed to make sure each extracted piece of metal is kept as is and checked for EM violations. The total transient simulation time is 900ns. Here the saved status at 800ns save800N.usim_25C@8.000000e-07 is reloaded. So essentially the simulation will be restarted from 800ns, and finished at 900ns. For the EMIR option, VAVO format is required for EM and IR-drop checks. The emir measurement will start at 801ns, and end at 900ns.

This example options setting is for final EMIR measurement. The options setting for status dump will be discussed later.

4.0 Flow and application details

In section 1.0, it has been discussed why average or RMS currents should be calculated for the EM check purpose under different circumstances. In section 3.2, we have mentioned that the power and ground parasitics may be aggressively reduced for the simulation to generate a status dump. Actually, it is even more efficient to short all the P/G nets in the simulation. The .usim_pn option of UltraSim gives us an easy way to achieve this. It should be noticed that the P/G nets will automatically be shorted by default for post-layout simulations if the sim_mode is not analog (a) or spice (s) [2]. Fig. 3 shows an example of UltraSim options setting where all the P/G nets are shorted and the status is saved at 800ns.

```
...
tran tran stop=800e-9

simulator lang=spice lookup=spectre
.usim_opt output_upper=0 ade=1 wf_spectre_syntax=1
.usim_opt wf_param_hier=1
.usim_opt sim_mode=a
.usim_opt wf_format=SST2
.usim_pn node=vdd method=short
.usim_pn node=vss method=short
```

```
.usim_pn node=vddio method=short
.usim_pn node=vssio method=short
.usim_save file=save800N.usim_25C time=800n
```

Fig. 3 An example of UltraSim options setting for status dump

There is an option *.usim_pn auto=yes method=short*, which claims to short all the P/G nets automatically for the post-layout simulation. But we found that this setting is not reliable, and may sometimes increase the runtime significantly.

In the following sections, the steps of the flow will be discussed.

4.1 Parasitic extraction to generate extract view

In section 2.0, the details of Assura RCX parameter selection have been discussed. Currently, VAVO/VAVEO accepts only the extract view output format from Assura RCX, and can only be invoked from the extract view display window. The highlight of violations is also carried out on the extract view display. Therefore the output format of Assura RCX must be the extract view.

It has also been pointed out that it is better to extract the P/G nets only for P/G EM and voltage drop checks. This strategy may save the runtime significantly with only a minor accuracy loss. In addition, if the purpose of the extraction is for IR-drop checks, an aggressive RC reduction may be chosen to further save the runtime during the phase 2 simulation.

4.2 Phase 1 simulation – generate a status dump

With the P/G only parasitic extraction and the UltraSim P/G short option, the simulation in phase 1 may be dramatically speeded up. In Fig. 3, it has been shown how to short P/G nets using some parameters of .usim_pn. An alternative approach is to carry out an aggressive RC reduction by UltraSim. For example, postl=3 may be used. The most aggressive reduction is postl=4. But it was found that setting postl=4 might cause some problems, resulting in a useless status dump.

It is obvious that the aggressive parasitic reduction is less effective than shorting P/G nets, according to the runtime reduction. But P/G nodes may sometimes be difficult to list completely. This alternative approach may provide designers with an easy way to reduce the runtime significantly.

The transient simulation time should be set long enough to make sure that the circuit can settle down before the end. A few indicator waveforms may be saved to verify this. At the end, a simulation status is saved for the phase 2 simulation to reload.

4.3 Phase 2 simulation – generate EMIR data file

Fig.2 shows the options setting for a phase 2 simulation. During the phase 2 simulation, the status dump saved at the end of the phase 1 simulation is reloaded by command .usim_restart, and .usim_emir command is used to generate binary EMIR data file which contains average/RMS/peak current values of all the parasitic resistors and average/RMS/peak voltage values at all the device P/G terminals. The parameters *start* and *stop* may be added to specify the

time interval for the current/voltage measurement. By reloading the status dump, the simulation actually starts from the time at which the status dump was saved, not from 0. Without start/stop parameter specifications, the default values will be 0 and the end of the whole transient simulation, respectively But the signal waveform data is not available from 0 to the time of saving the status dump. This will result in wrong EMIR data. Therefore, the parameters *start* and *stop* must be specified in order to generate correct EMIR data.

It should be emphasized that the input netlist used in phase 2 must be exactly the same as that in phase 1 to guarantee that the reloading works properly. If the two netlists are different, even just slightly different, the reloading may completely be out of order.

4.4 VAVO/VAVEO invocation to generate EM/IR-drop violation reports

For EM verifications, an EM data file is required, whose path should be the value of an environment variable _vsaEMDataFile. Other details can be found in the corresponding user guide [3].

Because the current version of VAVO/VAVEO is incapable of dealing with the area parameter for the current density of contacts and vias, the Current Density Milliamps Per Via keyword (currentDensityMPV) is introduced [3]. Fig. 4 is a relevant piece of the emDataFile.

```
…
viaLayers = ("CONT" "VIA1" "VIA2" "VIA3" "VIA4" )
viaWidthList = ( ( "CONT" 1 ) ( "VIA1" 1 ) ( "VIA2" 1 ) ( "VIA3" 1 ) ( "VIA4" 1 ) )
currentDensityMPV = T
xrefLayers = (
…
( "via1"                    ("VIA1" "VIA1"))
…
avgCurrentDensSpecList = (
(nil layer "VIA1" minW 0 maxW -1 res 3.5 currentDensity    ((1.0*0.326 , 85)
                                                            (0.63*0.326 , 100)
                                                            (0.48*0.326 , 110)
                                                            (0.32*0.326 , 125)
                                                            (0.25*0.326 , 135)
                                                             (0.18*0.326 , 150)))
…
```

Fig. 4 Part of an emDataFile related to vias

In the VAVO/VAVEO user guide [3], the value of currentDensityMPV is set to true, i.e. currentDensityMPV = true. It was found that VAVO/VAVEO did not accept it. But if it is changed to currentDensityMPV = T, it will work well.

In this current density specification list, 0.326 (mA) is the maximum current allowed per via, 85, 100, 110 through 150 are temperature numbers in centigrade, and 1.0, 0.63, 0.48 through 0.18 are the corresponding temperature de-rating factors.

It is suggested that if currentDensityMPV is set to T, the widths of all the contacts and vias be normalized, i.e. set them all to 1 as shown in Fig. 4. Thus the width of a contact/via element will represent the number of contacts/vias. This will make the EM violation report more understandable. One example report is shown in Fig. 5.

```
ELECTROMIGRATION ANALYSIS RESULTS

RESULTS FILE CREATED    = "Apr 24 09:09:51 2007"
PROGRAM VERSION         = 5.10.41.500.4.84 (10.1.1e)
DFII VERSION            = 5.10.41.500.4.84
ASSURA VERSION=3.1.6_USR1 SPECTRE VERSION=5.10.41.040507
ULTRASIM VERSION=6.0.2.164
SIMULATOR               = "ultrasim"
USER SUPPLIED VALUES:
   TOP LIBRARY NAME     = "testBench"
   TOP CELL NAME        = "ADC14D105_top_CMOS_test"
   TOP VIEW NAME        = "schematic"
...
-------------------------------------------------------------------
-
RESULTS AT "AVERAGE"
        Instance                        Measured  No of  Minimum  Current    Density
%Failed  Name          Layer   Current    Width    Vias    Width    Density    Limit
215.9%  rd24698        MET2    524u       0.32     NA      0.942    1.638      0.518
215.9%  rd24704        MET2    523.97u    0.32     NA      0.942    1.637      0.518
151.2%  rrvia1_22483   VIA1     524u         2       2      5.023    0.262      0.104
151.1%  rrvia1_22490   VIA1    523.97u       2       2      5.023    0.262      0.104
34.2%   re75045        MET1    278.61u    0.44     NA      0.581    0.633      0.472
33.7%   rrvia1_24225   VIA1    278.85u       2       2      2.673    0.139      0.104
33.6%   rrvia1_24228   VIA1    278.84u       2       2      2.673    0.139      0.104
...
```

Fig. 5 An example of VAVEO average current EM report

One may already have noticed that the value of the measured width of a via element is exactly the same as that of the number of vias. This is the result of the width normalization for contacts and vias. The value of the minimum width for a via element represents the number of vias required. If it is not an integer, it should be rounded up. For example, the number 5.023 should be rounded up to 6, i.e. the minimum number of vias is 6.

5.0 Case study

5.1 Example of an ADC design

This ADC circuit is a large AMS design with about half a million MOS transistors. There are hundreds of thousands parasitic resistors in its power and ground nets. The schematic simulation showed that the circuit needed more than 250 nanoseconds to settle down, and the analog simulation mode (sim_mode=a) was needed to get the desired convergence. With the total

transient simulation time equal to 350n and no parasitic reduction, it took more than 4 days to finish the job and to generate the EMIR data of 300ns through 350ns.

If the traditional VAVO/VAVEO flow was used, to achieve the similar level of accuracy, the waveform data needed to be set to use double precision floating numbers and the default speed = 5 needed to be changed to 3. The runtime would be increased to more than a week.

With the approach suggested before, the phase 1 simulation was done by shorting all the P/G nets and saving the status at 300ns. The total phase 1 simulation time took only several hours. In the phase 2 simulation, postl=0 was used to guarantee all the parasitic resistors were kept. The saved status was reloaded and the EMIR data was generated from 301ns to 350ns. The phase 2 simulation took a bit less than one day.

Compared to the traditional VAVO/VAVEO flow, the new approach saved the runtime dramatically, and achieved even better accuracy.

5.2 Example of a power regulator

This design has only a few tens of thousands transistors, but requires much longer time to reach the stable status (about 450 microseconds). With this much smaller design, it still took more than 4 days to get the final EM violation report if no parasitic reduction was done.

By adopting the flow described in this paper, the total simulation time was reduced to a bit more than one day. But some false violations were generated.

After a detailed examination, it was found that the false violations were caused by Assura RCX generated parasitic netlist. Some pieces of very wide metal were extracted as the parallel resistors with different widths. For the resistors generated from the same piece of metal, some were measured to have bigger current density values than the other. But if all the currents and widths were added together, there would be no violations. Another situation of false violations was that the width and length were swapped for some resistors with very small length to width ratios (less than 1). With the correct length and width values, no EM violations would occur.

6.0 Effectiveness and limitation discussion

As described in the previous sections and demonstrated by two real applications, the EM/IR-drop flow proposed in this paper may reduce the runtime significantly and achieve the same level of accuracy. For some large AMS designs, the direct EM simulation may be extremely difficult or impractical without the described improvements.

In addition, some false violations may be generated and may cause confusion for designers. These were mainly caused by the inadequate fractures of parasitic resistance. For example, some parasitic resistors had multiple widths, some had the width and length swapped. If these problems could be resolved, most false violations would have been gone.

7.0 Concluding Remarks

We have proposed an effective EM verification flow with UltraSim and VAVO/VAVEO. The selective parasitic extraction is featured with the power or ground nets extracted in the R-only mode for EM checks, and in the RC mode for IR-drop verifications. The two-phase UltraSim simulation part is carried out in such a way that the first phase is featured with the shorted P/G nets in order to generate a status dump, and the second phase starts by reloading the status dump. The .usim_emir command is used to generate the EMIR data file, and no parasitic reduction is done. This approach has resolved the long settle-down time problem, and has dramatically reduced the total runtime. The case study has demonstrated its feasibility and effectiveness.

For the future work, it is critical to reduce the number of false violations.

8.0 Acknowledgements

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9.0 References

[1] Cadence *Assura Physical Verification User Guide*, Product Version 3.1.6. September 2006
[2] Cadence *Virtuoso UltraSim Simulator User Guide*, Product Version 6.1, November 2006
[3] Cadence *Virtuoso Analog VoltageStorm and ElectronStorm User Guide*, Product Version 10.1, August 2006