Encounter Timing System

Unified timing analysis for faster design closure and signoff

Timing and signal integrity analysis can consume a significant portion of the overall silicon realization design cycle. Using Cadence® Encounter® Timing System with Encounter Digital Implementation System, design teams benefit from an advanced timing analysis infrastructure that tightly couples the design implementation environment with the timing signoff environment. This improves timing convergence throughout the design flow and greatly reduces the time to design closure. As a complete standalone solution, Encounter Timing System offers silicon-accurate timing signoff and signal integrity analysis that ensures operational chips after tapeout.

Encounter Timing System

Industry-endorsed and production-proven on both mainstream and advanced technology node designs, Encounter Timing System is a full-chip static timing analysis (STA) solution providing gate-level delay calculation, signoff-level timing and signal integrity (SI) analysis, statistical timing and leakage analysis, advanced on-chip variation analysis, and advanced node functionality required for double-patterning and waveform effects.

Designers have traditionally relied on one timing method for design implementation and a different timing method for signoff analysis. This leads to over-design with excessive timing margins and additional iterations in order to meet timing convergence throughout the place-and-route flow and correlation to timing signoff analysis at the end of the design flow.

Encounter Timing System removes the iteration bottleneck by providing a consistent, integrated Common Timing Engine for both the design implementation stage and the final timing verification stage of the design cycle. The result is correlation and convergence between implementation and signoff for faster timing closure.
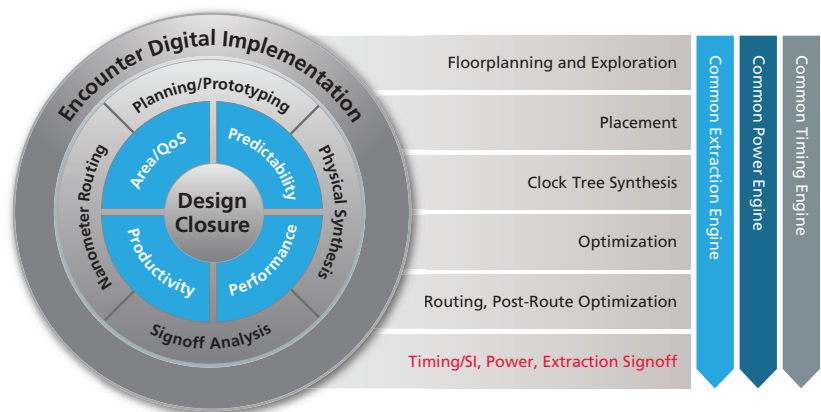

Figure 1: Unified timing for implementation and signoff provides faster design convergence and timing closure

Benefits

- Advanced timing solution with comprehensive analysis
  - Delay calculation
  - Static timing analysis
  - SI analysis
  - Statistical timing analysis
  - On-chip variation analysis
- Integrated with EDI System
  - Consistent timing analysis during implementation throughout the flow and signoff at the end of the flow

- Faster design convergence and timing closure with smaller design margin
  - Common database infrastructure for fast setup and a consistent usage model throughout the flow
- Unmatched timing signoff accuracy
  - Prevents excessive over-design to exceed performance, power, and area targets
  - Delivers accurate base delay and SI delay calculation to within 2-5% of SPICE

– Leverages current source models for greater accuracy on mainstream and advanced node designs
– Offers built-in critical path simulation for delay and SI correlation with SPICE

- Higher throughput for shorter design cycles and faster time to design signoff
  – End-to-end multi-threaded timing and SI analysis for faster signoff turnaround
  – Concurrent multi-mode/multi-corner (MMMC) timing and SI analysis for large view-count designs
  – Distributed multi-CPU and multi-threaded processing for maximum hardware utilization

- Higher productivity to shorten tapeout schedules by weeks
  – Industry-renowned global timing debug to accelerate root-cause and bottleneck analysis
  – MMMC-aware timing debug for quick timing issue identification across all views
  – MMMC signoff ECO optimization and repair across all timing views for fewer ECO cycles

- Supported by major foundries, ASIC, and IP vendors, and used exclusively by multiple IDMs for signoff

Features

Encounter Timing System provides a comprehensive timing analysis and signoff verification solution that includes automated signoff ECO, advanced modeling for precise delay calculation, power-aware static timing analysis (STA), accurate signal integrity (SI) crosstalk delay and glitch analysis, and statistical timing and leakage analysis.

Architected to address advanced node designs, Encounter Timing System realizes double-pattern effects using multi-value SPEF parasitics, considers complex waveform effects and back-miller current through proprietary modeling, and incorporates advanced on-chip and die-to-die variation effects with STA.

Encounter Timing System provides an intuitive set of GUI-driven debug interfaces for timing, clock, and SI, providing "what-if" analysis features to identify and eliminate timing and noise issues to speed the path to final tapeout.

Automated MMMC Signoff ECO

With the exploding number of multiple operating modes and multiple PVT corners for multi-million instance designs, the complexities of closing timing continues to be a major bottleneck in the design flow process. Designers need to manage the multiple views to be processed, execute distributed multi-mode/multi-corner (MMMC) static timing analysis (STA) on all the views, perform ECO optimization and repair, and close timing, within the target tapeout schedule.

With its unique MMMC infrastructure, Encounter Timing System can automatically execute distributed STA over multiple timing views. Then MMMC Signoff ECO can optimize the timing results for multiple ECO constraints over all MMMC views. The STA operation is dynamically kept alive for automatic identification of the best timing over all potential ECO repairs. The result is a physically implementable ECO file that eliminates all ECO violations in a single pass, without degrading other timing criteria.

A unique and differentiated feature of Encounter MMMC signoff ECO is the ability to generate a physically aware ECO file. Because Encounter Timing System is so tightly integrated with EDI System, access to the physical design enables timing optimization to create a 100% legalized ECO file for all buffer placements. This eliminates time-consuming rip-up-and-reroute iterations, placement legalization runs, and routing DRC checks that are required to create a fully legalized design after physical ECO changes. MMMC signoff ECO provides more than 30% improvement in overall design cycle time, compared to scripted, non-physically aware ECO methodologies.

Accurate crosstalk analysis

Encounter Timing System calculates the impact of crosstalk on the design by using a combination of cell- and transistor-level models. For noisy nets that exhibit the most non-linear behavior, Encounter Timing System incorporates an on-the-fly SPICE simulation engine to accurately calculate noise-on-delay effects. To maintain accuracy, a unique path-based alignment (PBA) technique is deployed to ensure realistic SI delay and glitch effects on critical timing paths. Without PBA, SI delay calculation can create an unrealistic and overly pessimistic worst-case path delay. Noise path pessimism removal (NPPR) finds the maximum noise delay change for the overall critical path, rather than for each individual net on the path.
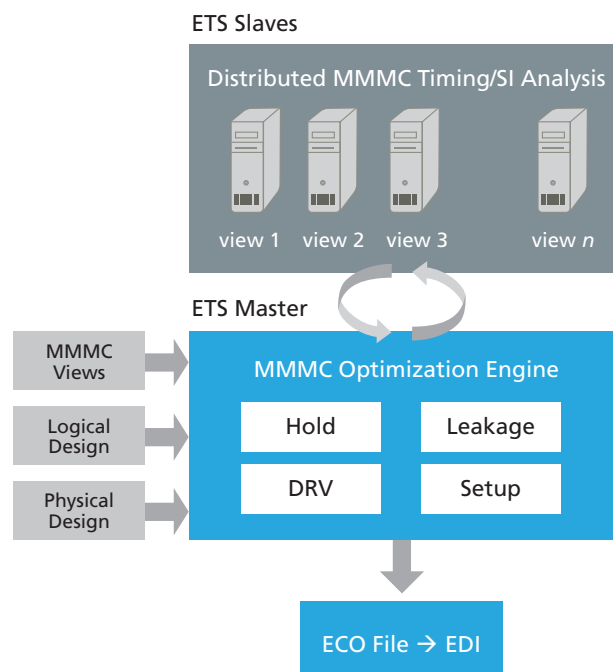

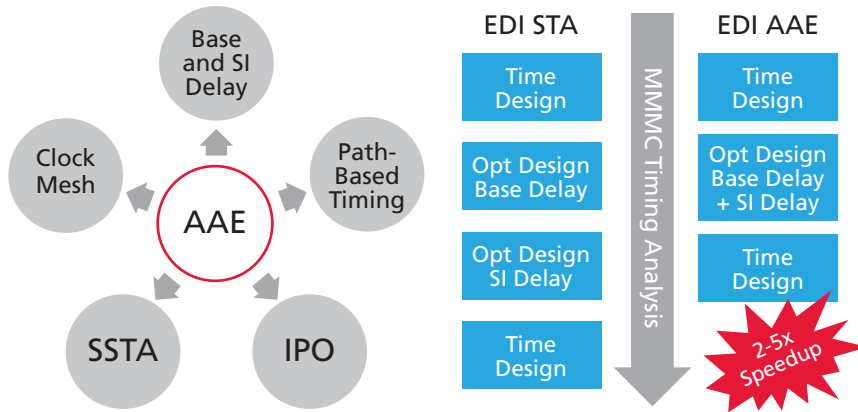*Figure 2: Automated MMMC Signoff ECO*

Figure 3: Fully integrated Advanced Analysis Engine provides unified timing calculation throughout the flow

Encounter Timing System also ensures functional validity by performing glitch noise propagation to register end-points and by ensuring that the register is not driven into instability. These unique PBA, NPPR, and glitch noise propagation capabilities greatly reduce the number of false crosstalk issues, which translates into much less work for place-and-route implementation and significantly fewer SI closure iterations.

Advanced Analysis Engine

Cadence provides an innovative, patent-pending technology with the Advanced Analysis Engine (AAE), which combines the typical two-step base delay and SI delay calculation into a single delay calculation step. AAE technology is also integrated into all aspects of timing analysis in EDI System and Encounter Timing System, applied to path-based alignment, in-placement optimization, statistical STA, and clock mesh analysis.

To address the capacity of today's multi-million instance designs, AAE is built from the ground up with a modern, multi-CPU and multi-threaded infrastructure, resulting in a very small memory footprint and a near linear 7x scalability on an 8-CPU machine.

Global timing debug

Global timing debug employs unique path visualization capabilities to determine the path's cause of failure. Selection of any timing path displays the details of a specific timing view with individual cell and wire delays, slack calculations of

skew, uncertainty and latency balancing, and hierarchical allocation. Constraint tracing is available through cross-probing to the SDC file to illuminate false-paths and multi-cycle paths.

Paths that share a common failure mode can be categorized dynamically, while continuing debugging on the remaining "non-categorized" paths. Categories can be visualized in the context of inter-dependent global timing to determine their priority and to determine which categories can be "fixed" in parallel. These visual categorization techniques can greatly reduce the number of iterations to obtain timing closure by intelligently debugging more than just the worst timing path.

Global clock debug

Encounter Timing System provides global clock debug for intuitive clock tree analysis that enables you to visually check, debug, and validate clock specifications providing a visual understanding of the clock tree structure, domain clock crossing, and buffer depth. Through interactive cross-probing between the schematic and the layout, insertion delay, skew, and transition time information can be examined.

Unified power analysis

Designers must also consider SI effects such as IR drop and crosstalk, and advanced low-power design techniques that use multiple voltage levels. Encounter Timing System provides a comprehensive static and dynamic solution for cell-level power analysis by integrating timing analysis with power analysis through the Common Power Engine. This integrated timing/power analysis environment delivers faster results. The Common Power Engine supports a vectored approach to achieve the highest accracy and a vectorless approach to enable accurate power analysis early in the design flow. .

Encounter Timing System accurately models the non-linear IR drop impact on timing to eliminate the inaccuracies of the traditional linear K-factor approach. The instance-based voltage data from the
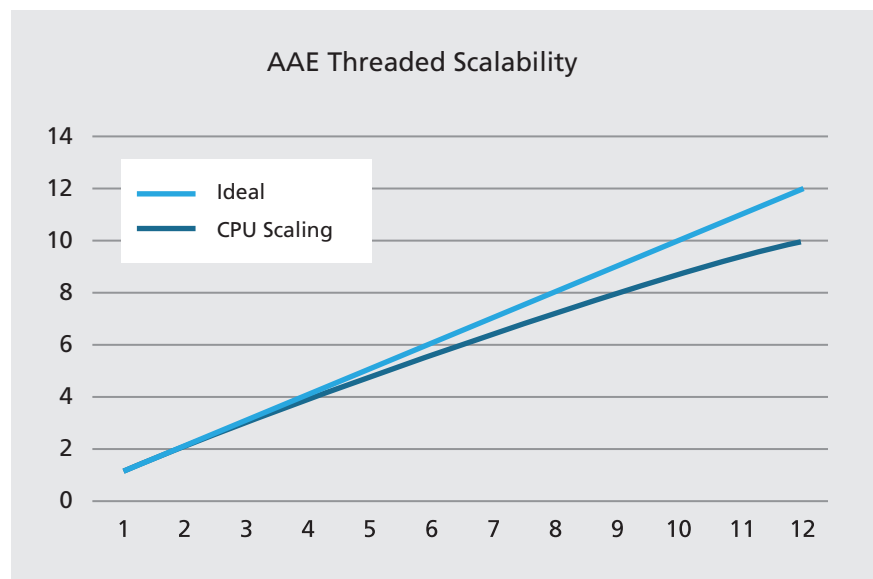

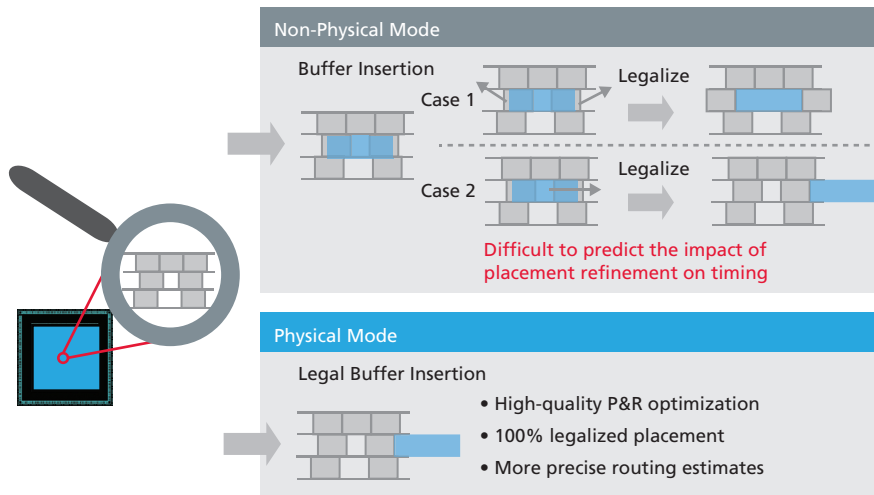Figure 4: AAE multi-threaded scalability, with more than a 7.8x speedup using 8 CPUs

Figure 5: MMMC Signoff ECO physical mode

Non-Physical Mode

Buffer Insertion

Case 1 — Legalize

Case 2 — Legalize

Difficult to predict the impact of placement refinement on timing

Physical Mode

Legal Buffer Insertion

• High-quality P&R optimization
• 100% legalized placement
• More precise routing estimates

Common Power Engine accounts for the effects of static and dynamic IR drop on path delays and signal integrity noise.

Low-power timing signoff

Encounter Timing System enables a simple flow where three libraries (called tri-libs) are characterized at three voltage points, which are sufficient to perform accurate non-linear delay calculation across a much wider range of voltage points. Encounter Timing System also supports the Common Power Format (CPF), which describes power intent throughout the design flow from system specification to tapeout.

Waveform effects on timing analysis

In advanced process technology nodes (at 28/20nm and below), the effects of coupling capacitance as ratio to wire ground capacitance are especially pronounced. As signal wires become closer, adjacent routing is relatively longer, creating additional aggressor cross-coupling capacitance to victim nets. As a result, the aggressor nets force more noise on the victim nets.

Today's timing cell models for advanced nodes are inadequate. Pin capacitance tables have very little data to extract miller capacitance. For example, a CCS only has 2 values. And an ECSM has 3 values. These cells are often charac-terized with narrow slew thresholds (e.g. 30-70), with no data available below the slew threshold. And slew rate is no longer adequate for parameterizing delay because different input waveforms with

the same slew lead to different delay values. As a result, slew measurements are ill-defined and inadequate to model the real downstream delay.

Exacerbated waveform effects from nonlinear receiver capacitance and back-miller current effects contribute to

"bumpy" victim net transitions that are not found in higher technology node designs. Back-miller current is caused by coupling capacitance between a victim net and the first stage of the receiver's output. The next stage acts as an aggressor to the victim net, causing a "bump" on the tail of the waveform, which has a strong impact on delay. In the worst case, a receiver without any load is switching very fast, which creates a strong back-miller current onto the victim.

To handle the waveform effects in advanced technology nodes, true waveform-based delay calculation is required. Cadence has a new patent-pending technology to model waveform effects, called equivalent waveform model (EWM), developed for Encounter Timing System.

To capture back-miller current effect, a current-source model-based simulation is applied to cell characterization, where a proprietary method of extracting the miller current from pin-capacitance models in CCS/ECSMs is applied. To determine the precise effects of cross-
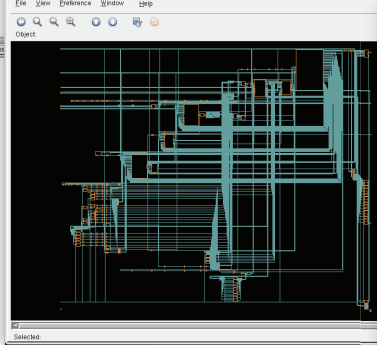
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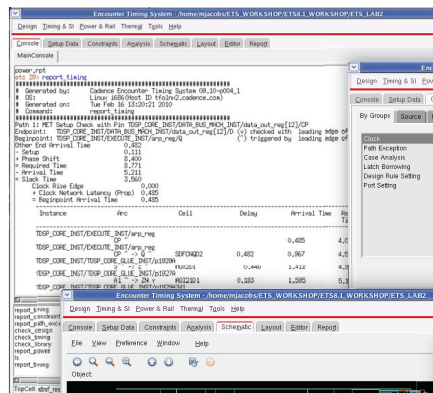
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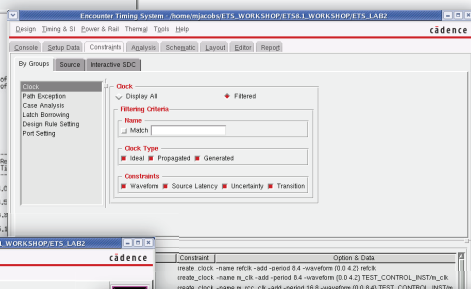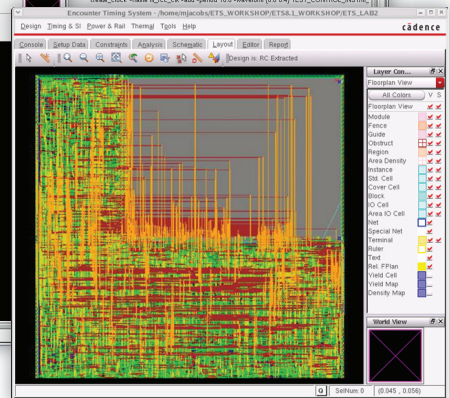
Schematic Viewer

Physical Viewer

Figure 6: Encounter Timing System user interface for intuitive design exploration

coupling capacitance on waveform propagation, a patented SI methodology that incorporates simulation-based full-stage delay calculation has been incorporated into AAE.

The results of Encounter Timing System with waveform propagation and miller current modeling dramatically improve the path measurement results to within 2-5% of SPICE.

Double patterning at 20nm

To capture the variation effects of double patterning at 20nm, Encounter Timing System incorporates multi-valued SPEF parasitic extraction results for minimum and maximum capacitance values from Cadence QRC Extraction. The SPEF file is read into the binary database to greatly improve parasitic value read time by, in some cases, as much as 120x. For setup timing analysis, Encounter Timing System traces the launch path through the late path and assigns the maximum capacitance value from the parasitic database, while the capture clock path is traced through the early path and is assigned the minimum capacitance value. For hold timing analysis, Encounter Timing System traces the launch path through the early path and assigns the minimum capacitance value from the parasitic database, while the capture clock path is traced through the late path and is assigned the maximum capacitance value. With minimum and maximum parasitics applied to setup and hold timing, rather than typical parasitics, Encounter Timing System can accurately simulate complete timing and SI results for 20nm designs.

Statistical static timing analysis

Traditional timing analysis accounts for process variations by introducing more aggressive guardbanding and by using multiple analysis corners to model different process and environmental variation combinations. This corner-based approach can be overly pessimistic since it reports timing scenarios that have an extremely small likelihood of occurring. Plus, the exponential growth in the number of corner combinations with the increasing number of parameters makes analysis on every corner impractical.

Statistical leakage power analysis

Encounter Timing System Statistical features include:

- Intra-die, die-to-die, and random variation support
- Block-based and path-based modes
- Consideration of crosstalk noise and leakage power impact
- Standardized S-ECSM library models and characterization support
- Consistency and integration with EDI System to automatically fix variation issues

Platforms

- Linux: 32-bit, 64-bit
- Sun Solaris: 64-bit
- IBM AIX: 64-bit

Standard Interface Support

Inputs

- Verilog, .lib, SDC, SDF, SPEF, Tcl
- Optional: ECSM, cdB, DEF, CPF, OA, VCD, OCV
- SSTA: statistical ECSM (S-ECSM), statistical SPEF (S-SPEF), statistical parameter distribution file (SPDF)

Outputs

- Timing reports, SDF, DRV report, power reports
- Packaging

- The Encounter Timing System L base license is available for basic timing analysis
- The Encounter Timing System XL base license is available for basic timing analysis and SI timing analysis
- The Encounter Timing System GXL Advanced Analysis option license is available to enable:
  - Statistical static timing analysis (SSTA)
  - Statistical static timing analysis (SSTA) with SI
  - Litho-aware timing
  - Statistical leakage power analysis (SLPA)

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