cadence®

# Cadence Chip Optimizer

## Manufacturing-aware full-chip modeling and layout optimization

Cadence® Chip Optimizer is a silicon-proven, full-chip physical design optimization system that improves manufacturability, yield, and performance. It addresses today's requirements for shorter time to convergence and time to volume. Cadence Chip Optimizer works seamlessly with the Cadence Encounter® digital IC design platform and the Virtuoso® custom design platform.

### Cadence Chip Optimizer

Cadence Chip Optimizer provides unique interconnect optimization capabilities that improve yield, manufacturability and timing closure during design. It optimizes layout based on electrical constraints, manufacturing rules, and objectives.

Used after conventional place and route in digital design flows, such as the Cadence Encounter digital IC design platform, Cadence Chip Optimizer improves timing, yield, manufacturing and performance of the largest designs. It also plays an important role in the interconnect design process for semi-custom design flows, such as the Cadence Virtuoso custom design platform.

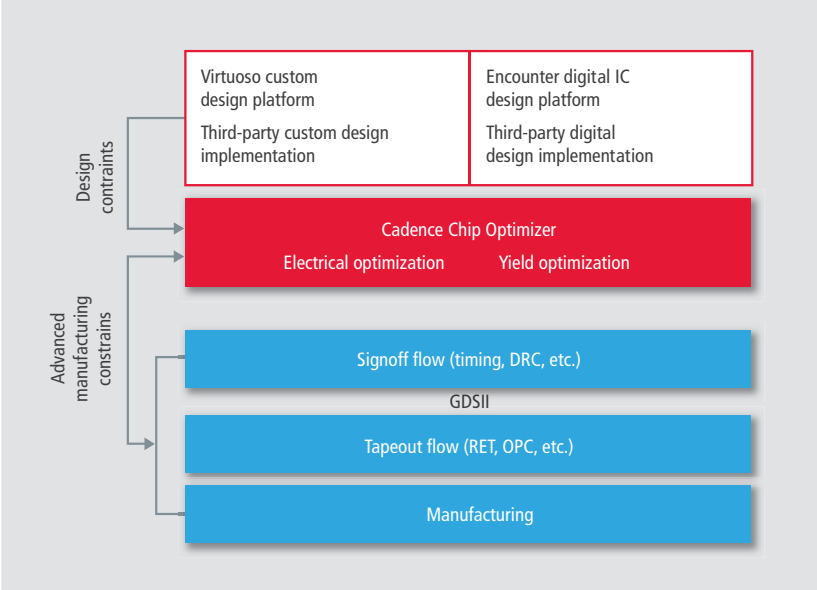


*Figure 1: Cadence Chip Optimizer*

### Innovative Space-based Architecture

Conventional IC implementation tools create an oversimplified model of the interconnect and associated foundry process rules. Cadence Chip Optimizer uses a patented three-dimensional, space-based approach to model and analyze true shapes and intervening physical spaces. It allows shapes and spaces to be positioned in the exact configuration and location required to correct sub-wavelength manufacturing effects. This capability affords greater precision and flexibility when optimizing the interconnects while using tiered design and manufacturing constraints.

### Manufacturing and Design Closure

Manufacturers and designers have different objectives. Fabs want designs to adhere to design for manufacturing (DFM) and design for yield (DFY) rules and recommendations for their advanced process nodes. Designers

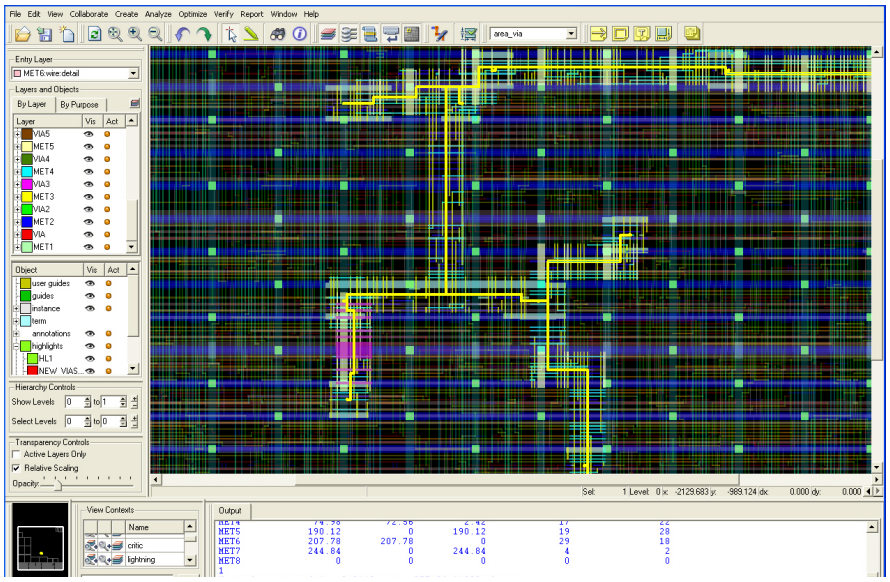

*Figure 2: Cadence Chip Optimizer improves manufacturability and performance by optimizing interconnect layers*

want to achieve the greatest performance while performing the least amount of guard-banding. Schedules and predictability are also paramount concerns for designers.

A common misconception is that these manufacturing and design objectives are always in opposition. However there is often a mutually agreeable solution. By optimizing wires (space and width), for example, designers can reduce the probability of opens and shorts (which is good for yield) while also reducing coupling capacitance (which is good for signal integrity, timing and power).

With the powerful analysis and topology optimization capabilities provided by Cadence Chip Optimizer, designers can quickly achieve convergence that addresses both manufacturing and design objectives.

## Benefits

- Addresses both DFY and DFM issues much earlier in the design flow
  - Faster geometric, electrical, and manufacturing convergence
  - Improves design margins and reduces guard-banding
  - Electrically (e.g., timing) correct design eliminates convergence iterations
  - Faster, more reliable ramp to volume silicon with up to six points of yield improvement
- Innovative approach handles the most sophisticated geometries and constraints
  - True hierarchical, three-dimensional space-based approach enables accurate and precise modeling and optimizations
  - Architected to handle complex and tiered rules and constraints from 90nm and below
  - Powerful topological changes ensure greatest manufacturability and performance gains
- Silicon proven
  - Proven on high-volume and high-performance silicon at 130, 180, 90, and 65nm process nodes
- Easily adopted
  - Works seamlessly with the Cadence Encounter and the Virtuoso platforms
  - Works with third-party implementation flows through industry-standard interfaces
  - Runs natively on OpenAccess

## Features

### Manufacturability and yield enhancements

- Optimizes vias to reduce via failures due to process window variability or misalignment. Enhancements include total via count reduction, adding multiple vias, optimizing enclosures and spacing
- Optimizes wires to reduce wire failures due to isolated lines (opens) or minimum spaced lines (shorts)
- Optimizes metal to minimize chemical mechanical polishing (CMP) effects
- Eliminates process antennas
- Increases manufacturability and RET efficiency by optimizing wire topologies

### Design closure enhancements

- Connectivity and design rules are omnipresent for correct-by-construction editing
- Wire push capability “pushes” neighboring wires to optimally fit a new wire and still meet design rules
- Improves design margins and reduces guard-banding
- Reduces total and coupling capacitance inline with timing and power objectives
- Power and ground optimization

### Unparalleled speed and capacity

- Offers speed and high-capacity through the use of new (patented) hierarchical modeling and search algorithms
- Multithreaded operation

### Fully integrated check and analysis

- Supports sophisticated recommended rules and constraints from 90nm and below
- Fast and accurate interactive DRC and connectivity (open/short) checking
- Browser to analyze optimization and verification results
- Critical areas (defect limited yield sensitive areas) are identified using critical area analysis techniques

### Full-featured navigation system

- Aerial view window provides full-chip navigation context
- Query engine enables powerful searches of layout data
- Designers can fully tune the desired layers, layer-purposes and transparency for display and selection
- Useful views and environment contexts can be bookmarked and saved

### Easy to learn, use, and extend

- Provides an intuitive windowing system and command set
- Extensive TCL programming interface

## Specifications

### Inputs

- OpenAccess, XML, LEF DEF, GDSII, CDB, SPEF, Timing Libraries and Constraints

### Outputs

- OpenAccess, XML, LEF DEF, GDSII

### Platforms

- Sun Solaris (32-bit, 64-bit)
- Linux (32-bit, 64-bit)
- IBM AIX (32-bit, 64-bit)

## Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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