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Cadence Space-Based Router, the next generation

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The Cadence Space-based Router won the EDN 17th annual Innovation Award last month. Cdnusers interviewed Stan Chow, Cadence VP of R&D for the Catena Project, about the router.

cdnusers: Tell us about your background working with the Cadence Space-Based Router.
Stan: I am running the R&D group developing Cadence Space-based Router and Cadence Chip Optimizer. I joined Project "Catena" mid way in their incubation program which started about 5 years ago. I knew several people in the group as we developed the Cadence Chip Assembly router in the 90's. We developed what we called the shape-based router, originally intended for PCB application, in Cooper & Chyan Technology which was acquired by Cadence. The IC-version of the router was used for chip assembly and device-level routing. CSR covers a wider spectrum of applications because of a better architecture and higher capacity.

cdnusers: Congratulations on winning the EDN 17th Annual Innovation Awards for the Cadence Space-Based Router. Tell us the one new thing designers should know about this Router.
Stan: You can consider the space-based router the next generation of shape-based router. It is the new architecture that enables a multitude of features and offers tremendous more values to customers.

cdnusers: Tell us how this feature works.
Stan: The space-based architecture offers much faster shape look-up and space look-up in a hierarchical and thread-safe environment, and it takes up much less memory. It is built for not only the router. It is generic enough to support a variety of applications, most notably DFM analysis and optimization. The space-based architecture allows us to handle a much bigger amount of data which is important as bigger designs are put into smaller dies in advanced processes.

cdnusers: Now tell us about a couple more features that users will find helpful when using the Space-based Router.
Stan: The space-based architecture enables many routing features. Understanding advanced process rules in 65/45/32nm processes is a key to Cadence Space-based Router. We need fast shape look-up and boolean operations to accurately look at the effective width and edge lengths of overlapping shapes, and measure against neighboring shapes with process and yield spacing rules in mind. We need to perform such operations hierarchically in custom designs where data is typically spreaded out in multiple levels in the hierarchy. Multi-threading is a 'must' to handle large

designs and take advantage of multi-way machines that are getting more and more popular. The Space-based Router works with Cadence Chip Optimizer, a DFM optimization product, and extractor by sharing data in the common architecture.

cdnusers: Now some personal questions. How do you concentrate when working? Any tricks?

Stan: Besides managing the two products, I provide technology to other product groups and work with selective customers on special collaboration projects. There are always plenty of issues and over a hundred emails every day. The key is to stay focused on high priority issues. Also don't get drowned by tactical issues and reserve time for strategic planning.

cdnusers: Where do you do your best thinking?

Stan: It usually happens when I have some quiet time, like when I drive, take a walk, or wait for a plane. Sometimes it happens when I bounce ideas off from colleagues.

cdnusers: What do you do after a long day or week of working on router problems to relieve your stress levels?

Stan: Go home and spend time with my family. They can always keep my mind off work.

About the author

Stan Chow is VP of R&D, Catena Group, at Cadence. Stan joined ECAD/Cadence in 1988 and has worked at Cadence the majority of the time since 1988. He works out of the Los Gatos, California office.

Stan obtained his BS and MS in EECS from UC Berkeley. His favorite outdoor activities include hiking, biking, soccer and traveling.