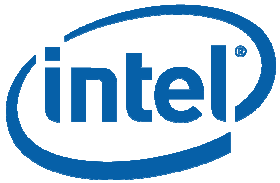


Dynamic IR-drop Analysis with VoltageStorm Dynamic Gate (VSDG) using different Power Grid Views for Cell Modeling

Steffen Kosinski

Intel GmbH

Disclaimer

This presentation deals with different power grid views for cell modelling in Cadence VoltageStorm. Test case analysis results are provided for informational purposes only. This presentation covers different methods to use the tool. This material does not imply any implicit or explicit preference statement or assessment on the quality of the tool.

Agenda

- Introduction
- Dynamic vs. Static IR-drop Analysis
- Power Grid Views
- VSDG IR-drop Analysis Results
- Conclusion

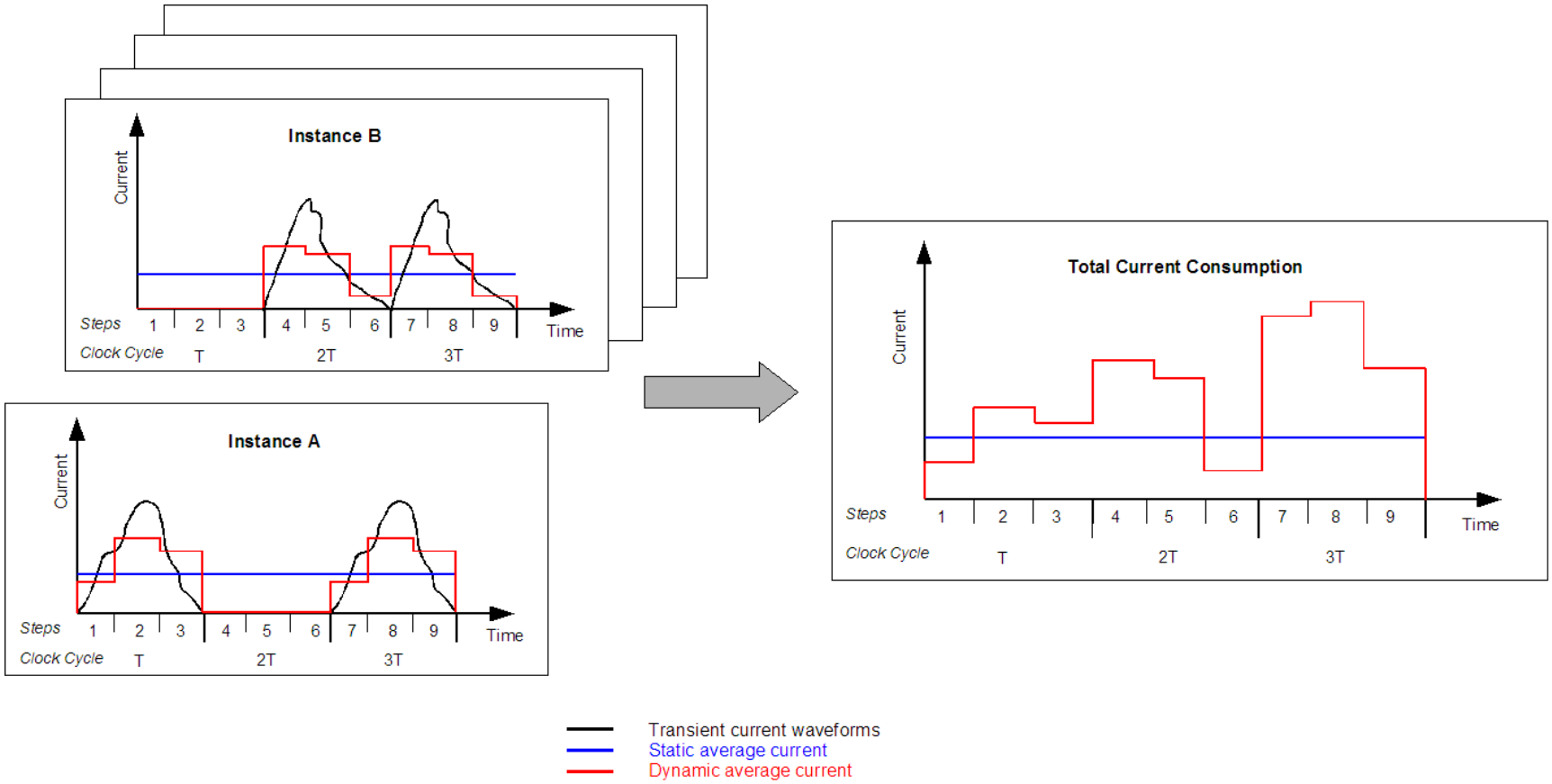
Introduction

- Steffen Kosinski – EDA Engineer at Intel GmbH in Braunschweig
- Diploma Thesis: Evaluation of Dynamic vs. Static IR-drop Analyses
- Currently: RV expert in European DA team for Intel projects in EMEA

- Our team:
  - Support Center for chip design teams in EMEA
  - Global Excellence Center for RV, SI and DFT
  - Part of Digital Enterprise Group (DEG) – Intels largest business group

- Intel Braunschweig:
  - Intel Germany Research Center
  - Microprocessor Lab Germany
  - Architecture and Planning
  - Design Automation and Support

Dynamic vs. Static IR-drop Analysis



Dynamic vs. Static IR-drop Analysis

Static approach

- Based on static average current
- Fast validation on high abstraction level
- Basic robustness check: open circuits, missing or insufficient vias, current density violations, insufficient power rail design

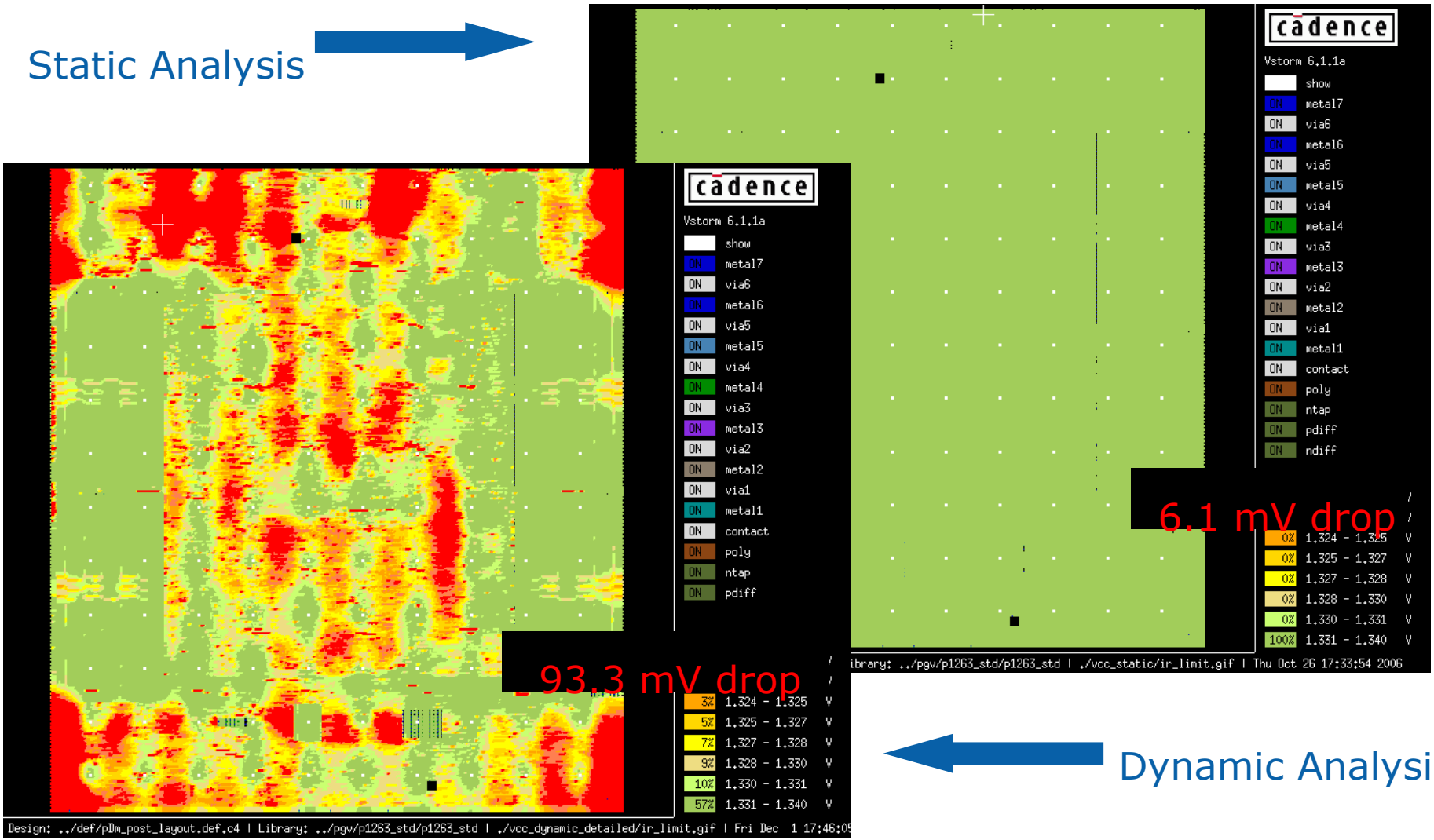
Dynamic approach (in addition to static)

- Based on PWL current waveforms
- Peak IR-drop detection due to Simultaneous Switching Noise (SSN)
- Additional analysis of the dynamic parasitic load on the supply net
- Captures dynamic behavior of circuit elements
- Enables effective decap cell placement

  - ➢ More accurate cell models needed
  - ➢ Longer runtimes and increased memory consumption

Dynamic vs. Static IR-drop Analysis

Static Analysis



Dynamic Analysis

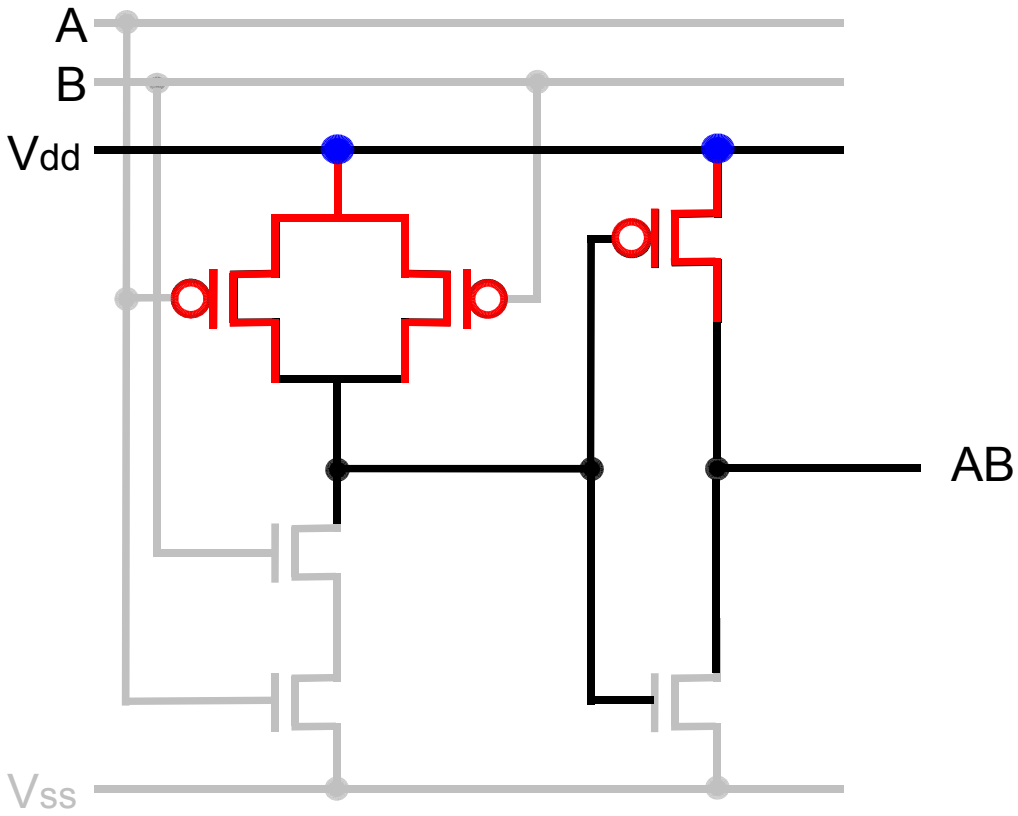
Power Grid Views

- Port view
  - Only ports connected to power grid
  - No information about internal topology
  - (Capacitances from detailed view)
- Quick detailed view
  - Only one tap current per node
    - Reduced R-network for internal representation
  - Capacitances from detailed view
- Collapsed view
  - Suppression of small tap currents
    - Reduced R-network for internal representation
  - Capacitances from detailed view
- Detailed view
  - Tap current for every device directly connected to the supply grid
  - Internal representation via RC-network

Higher abstraction level

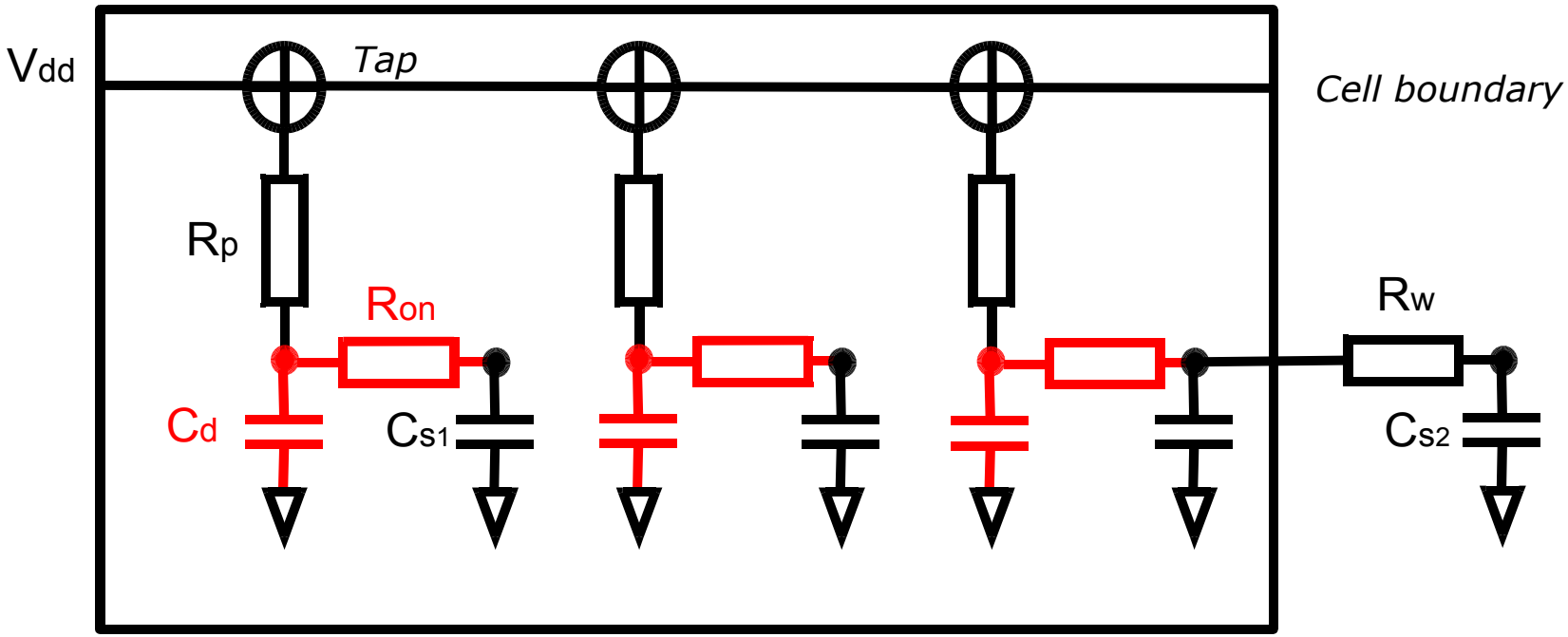
Power Grid Views

Example: AND-gate



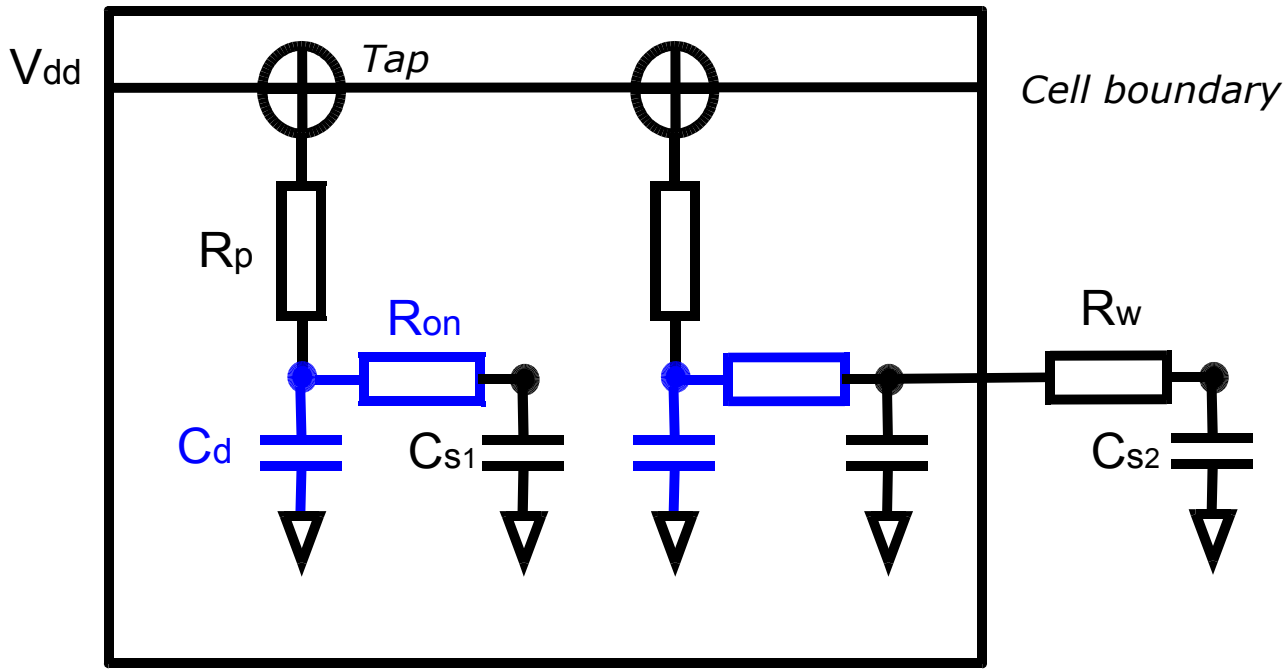
Power Grid Views

AND-gate Detailed View / Collapsed View CRC Model



Power Grid Views

AND-gate Quick Detailed View CRC Model



Power Grid Views

Number of Taps (Vdd)

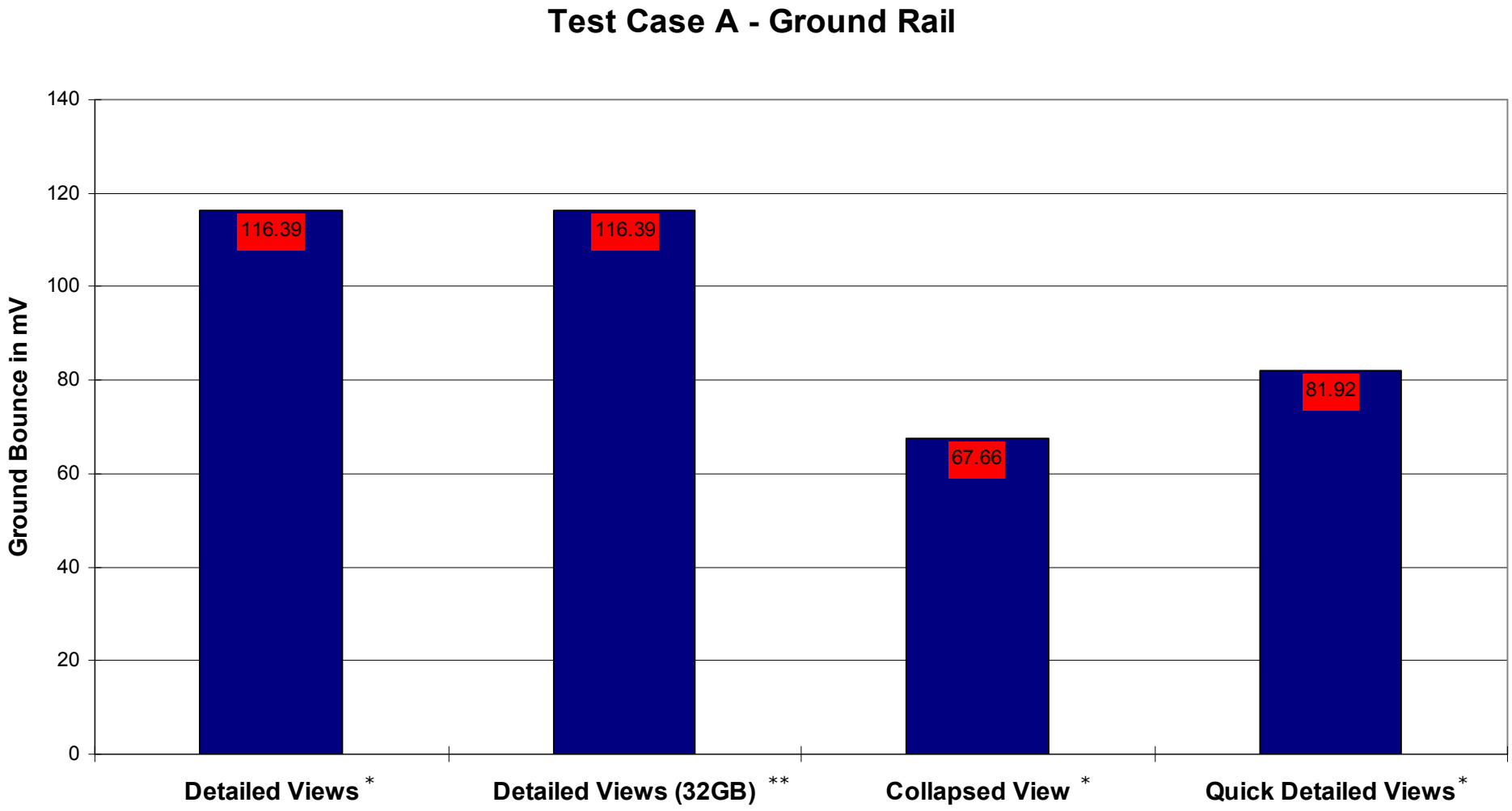
Cell	Detailed	Collapsed	Quick Detailed	Port
Inverter	1	1	1	1
AND	3	3	2	1
160x16 reg	12094	1122	7219	124
204x60 reg	61616	28980	49754	600
128x84 reg	97342	62738	75841	2120
1024x16 ROM	3444	1575	2630	68
4096x66 SRAM	590412	559251	46486	1326

VSDG IR-drop Analysis Results

Test-Cases

- Test Case A:
  - 90 nm design
  - Standard cells, register modules
  - Memory modules (1024x16 ROM and 4096x66 SRAM)
  - Size: 41.2 mm²
  - 193 079 instances
- Test Case B:
  - 65 nm design
  - Standard cells
  - Large register modules
  - Size: 17,2 mm²
  - 1 072 133 instances

VSDG IR-drop Analysis Results

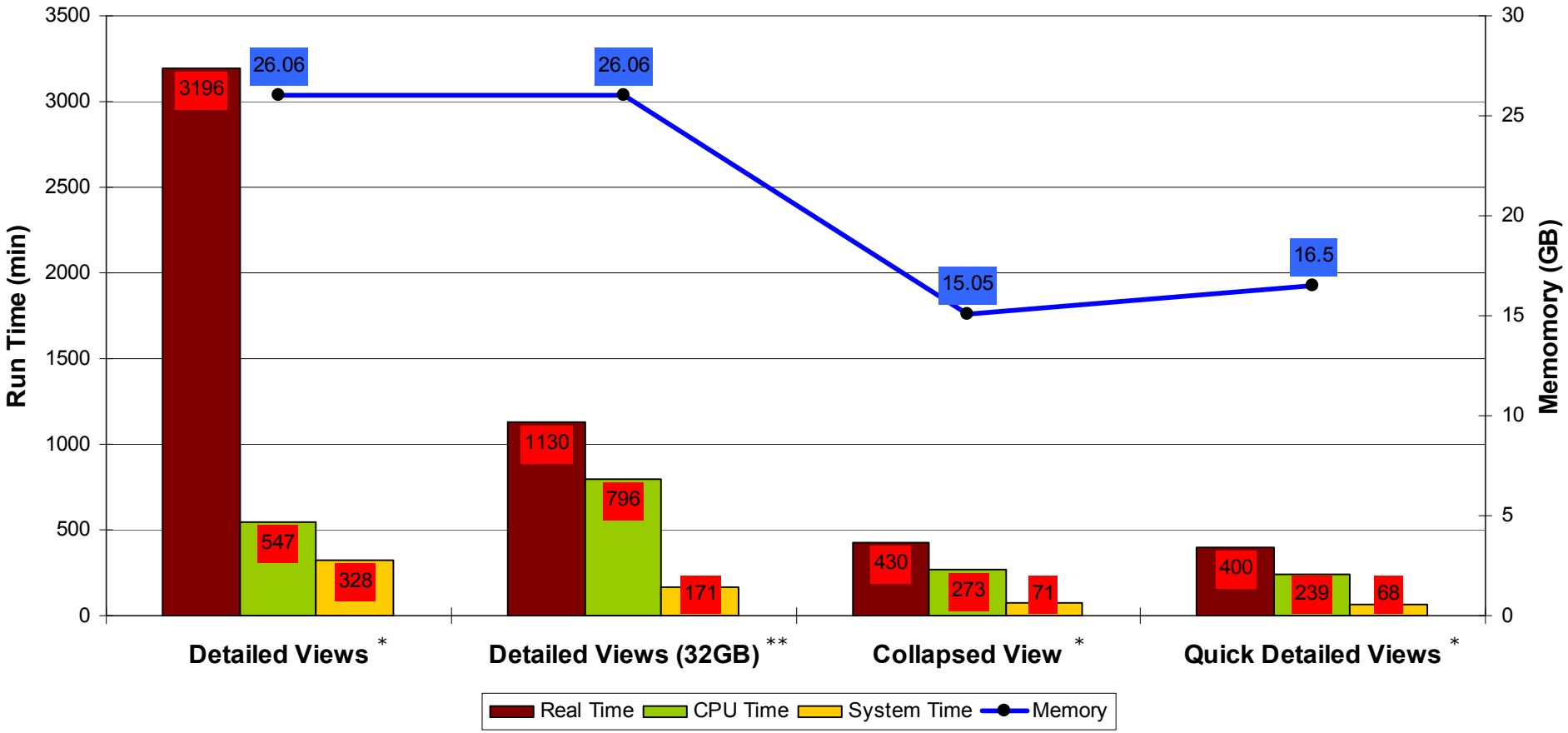


* 3.8 GHz Intel® Xeon™ machine with 16GB RAM

** 3.66 GHz Intel® Xeon™ machine with 32GB RAM

VSDG IR-drop Analysis Results

Test Case A - Run Times and Memory Consumption (Ground Rail)



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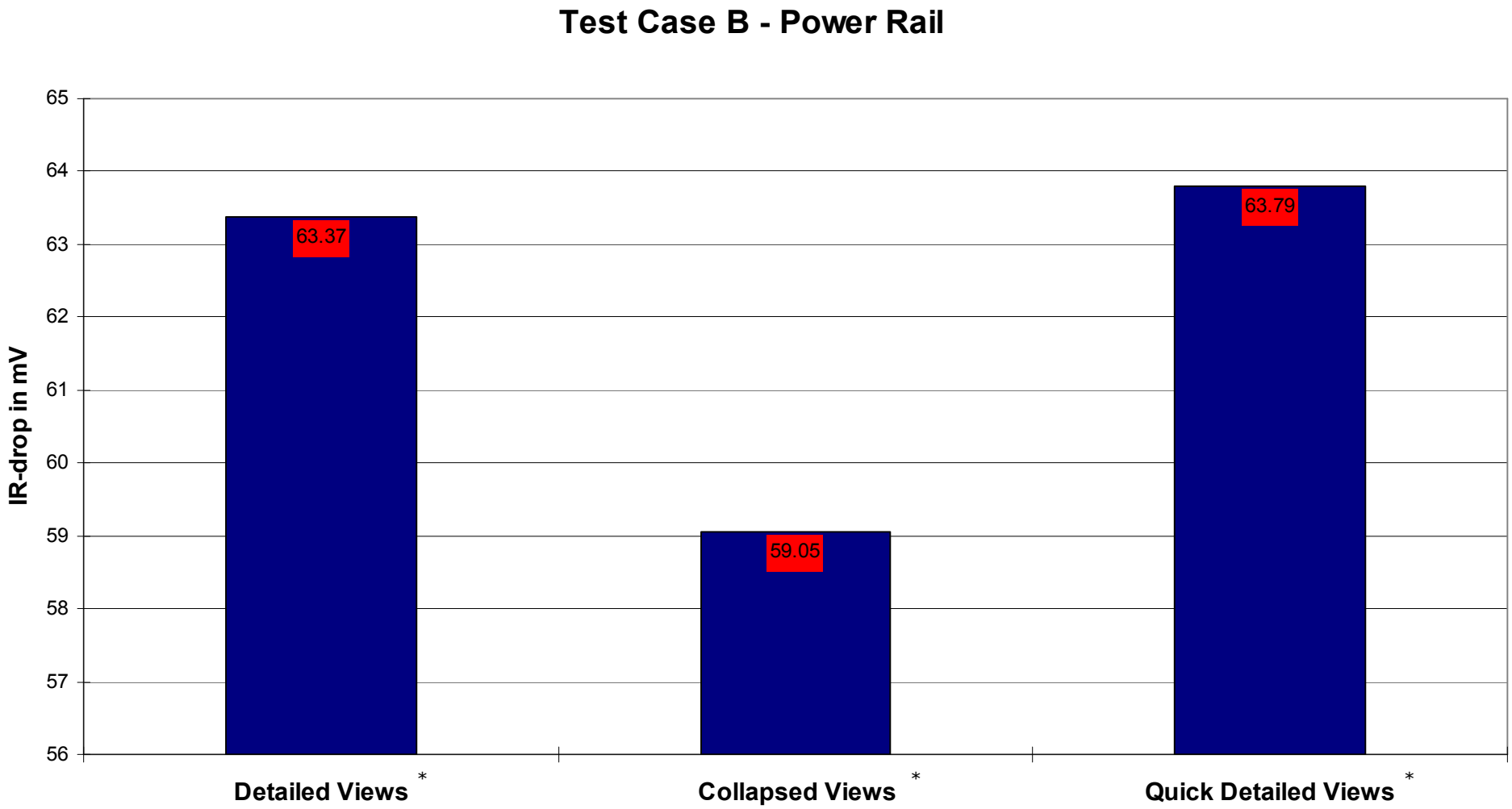
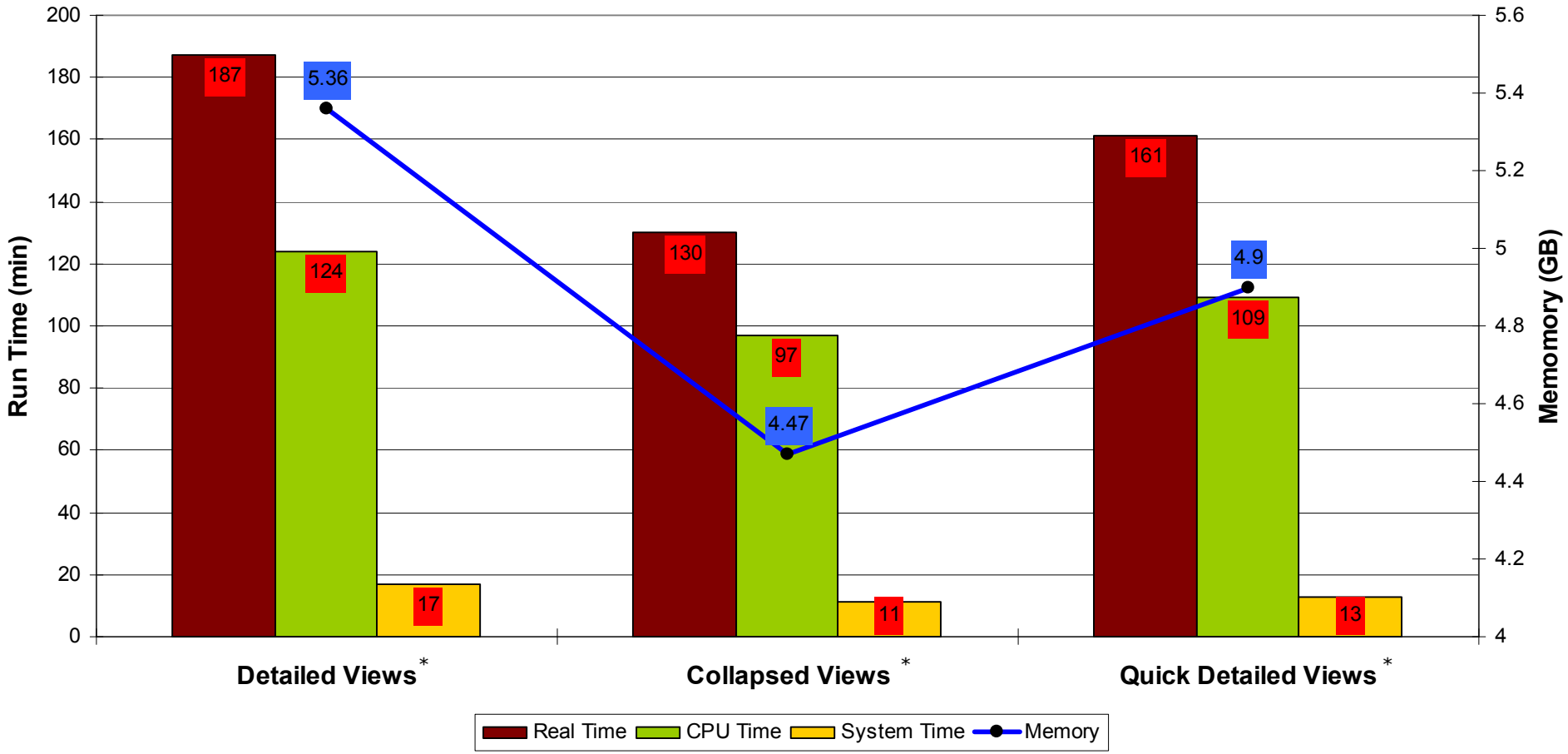
VSDG IR-drop Analysis Results



* 3.8 GHz Intel® Xeon™ machine with 16GB RAM

VSDG IR-drop Analysis Results

Test Case B - Run Times and Memory Consumption (Power Rail)



* 3.8 GHz Intel® Xeon™ machine with 16GB RAM

Conclusion

	Weight	Detailed View	Collapsed View	Quick Detailed View
Test Case A Run Time	1	1	4	5
Test Case A Memory	1	1	5	4
Test Case A Accuracy	2	5	2	3
Test Case B Run Time	1	3	5	4
Test Case B Memory	1	3	5	4
Test Case B Accuracy	2	5	3	4
Total Rating		**28**	**29**	**31**

Rating: 5 = best, 4 = good, 3 = medium, 2 = poor, 1 = unaccaptable

Conclusion

- Usage of Collapsed or Quick Detailed Power Grid Views increases dynamic analysis performance
- Performance improvement depends on the design
- Higher accuracy with Quick Detailed Views compared to Collapsed Views

- Collapsed Views are generated together with Detailed Views
  - ➢ No additional effort needed
- Quick Detailed Views need an additional generation step after Detailed View generation

- **Quick Detailed Views provide best trade-off between accuracy and performance improvement**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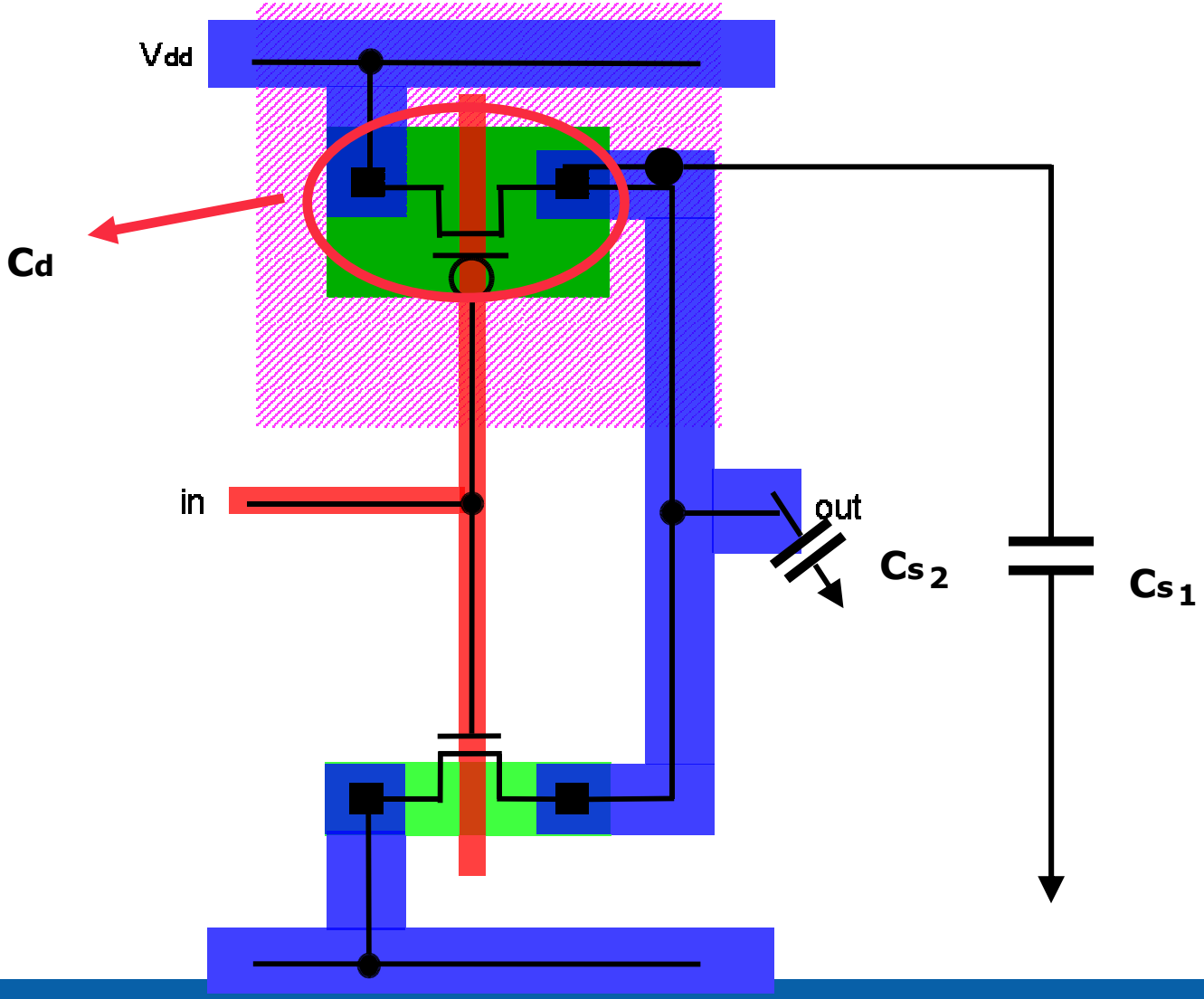
Backup

Power Grid Views



Power Grid Views

Detailed View CRC Model