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Interview: Freescale's Alejandro uses Encounter Timing System to Overcome Timing Challenges

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Freescale's Alejandro Albuerne uses Encounter Timing System to Overcome Timing Challenges

Static Timing Analysis (STA) is a very critical and important part of the design sign-off process. cdnusers interviewed Alejandro (Alex) Albuerne from Freescale Semiconductors to find out how Encounter Timing System (ETS) helped solve and debug timing challenges in Freescale's sign-off process. Alex has responsibility for the sign-off and delay calculation phases of Freescale designs in Munich.

cdnusers: Alex, tell us about Freescale Semiconduct and the products you develop.

Alex:Freescale Semiconductor is a global leader in the design and manufacture of embedded semiconductors for the automotive, consumer, industrial, networking and wireless markets. In my department, we are concentrated in microprocessors and microcontrollers for the automotive branch.

cdnusers: What process node are you using, and what are the specific challenges you see at this node or beyond?

Alex: Although the company has products in several process nodes, the products that my team develops are done, at the moment, with the 180nm and 130nm technologies. The change from 250nm was not especially dramatic. First, SI problems, more leakage, but nothing especially difficult to achieve. We plan to jump into the 90nm process node this year, so more serious SI and leakage problems are expected.

cdnusers: Can you give an example of some of those problems?

Alex: My first design with the 130nm technology was especially SI sensitive. There were a lot of SI problems on the pads and it was a little bit difficult to achieve timing. This was for me the first contact with SI problems in a design. Anyway, as I explained in the answer to the prior question, at the end these problems were not difficult to solve.

cdnusers: What tools do you use in your flow?

Alex: For more than a year, we are using a complete Cadence flow (RTL to GDS2) for our designs. RC-RTL compiler is used for synthesis; CCD (Conformal Constraint Designer) for constraints design; Encounter for placement, routing, optimization and STA; Fire and Ice QRC for extraction, etc.

cdnusers: How do you use Encounter Timing System?

Alex: Till now, I haven't used ETS for any sign-off. All our tapeouts were done using Encounter in CTE (Common Timing Engine) mode without loading LEFs. Since this is a new tool, I'm currently working on the setup of it for our next proyect but I can say that there are not too many differencies between the setup of ETS and CTE, so the change is easy and I don't expect any new problems.

cdnusers: Then, how did you use CTE for your designs?
Alex: As Cadence recommended, we load the design only with lib files and without DEF and LEFs. Signoff is done with the SPEF parasitics files coming from the QRC tool. Since there are many modes and corners in our designs, I used to load several sessions to analyze all possible clock propagations and corners. In our last project, I used for the first time the MMMC (Multi-mode Multicorner)possibilities of Encounter to save time and memory. I can say that this is a great feature and allows the designer to have several functional and test modes visible at the same time, so timing problems are easily solved. It's really helpful to see the impact of a cell sizing in all modes and corners at the same time.

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We generate SDFs with CTE too.

cdnusers: What challenge does ETS solve for you?
Alex:Since CTE and ETS are similar, I think I can answer this question with my knowledge about CTE. Signoff requires a quick and easy to understand tool. Although it was difficult to have it under control at the beginning (changing tools is always a challenge), with the help of the Cadence team, we could do our first tapeout with a complete Cadence tool flow last year. Big issues were: the check of data-to-data checks, problems with SDF (Standard Delay Format) generation and some clock propagation issues. After hard work, we were able to do STA analysis and signoff for the first time with Cadence CTE. Now we use the tool without problems, loading multiple modes and corners at the same time, allowing data-to-data checks for synthesis and STA, doing SI-incremental-SDF analysis, etc.

After my first steps with ETS, I've seen that all the STA positive things of CTE are there, but now debugging is easier thanks to the new GUI and path analysis options. With ETS it is easy to set MMMC, size cells and see impact on timing for all modes, change constraints and check what happens, etc. One important feature is the possibility to call CCD (Conformal Constraints Designer) to check constraints or do false-path analysis. For @speed tests, we need a huge amount of critical

paths, but some of those paths are impossible to simulate and therefore the coverage falls. With CTE and CCD, we are able to generate paths, load them in CCD, check them and generate false paths for those that are impossible to simulate (SDC file), load the new SDC in CTE and generate a new set of critical paths with a less % of false-paths. This is done with a script that 'jumps' between the two tools and allows the user to generate a better set of paths automatically.

cdnusers: What do you like best about ETS?

Alex: I think that the MMMC options and the possibility to call CCD from the tool are two great features of ETS. It's really helpful and saves a lot of time, while having all the information at the same time in only one session. In the past, we had several licence problems when several teams were working on several sign-offs. Many modes and many corners and one session for each corner multiplies the amount of required licences at the same time. Now, with MMMC, each designer can have all his modes and corners at the same time, saving time and licences. In the other hand, CCD allows us to have a better set of paths that increase the @speed coverage.

There is another interesting feature in ETS that allows the user to group paths and debug timing. I've only used it to test the tool, but it looks like a useful and important feature to debug timing in complex designs in the future. Timing violations can be grouped and debugged separately, so the designer will have a better view of the real problems of the design. Old tools only reported a mess of violations, ETS allows you to separate them easily to better understand what the real problems are.

cdnusers: How many tapeouts do you expect to do this year using ETS for signoff?

Alex: Sorry, but I can't answer this question. I can only say that since we work with a Cadence-only flow, the rate of signoffs didn't change.

cdnusers: What do you like best about ETS?

Alex: Give it a try. Some designers think that ETS is not yet a 'good enough' tool for signoff, but I think they will be surprised if they try to use it on their designs. I was pleasantly surprised for a year and now the tool is much better and has many new features (MMMC, data-to-data checks, stand-alone environment, CCD, etc.). Changing a tool is always difficult; the user 'thinks' in the way of the old tool and at the beginning is complicated to adapt his mind to the new environment and all looks like 'old times were always better'. But after a few changes and a little bit of effort, its easy to set the tool correctly and see that ETS is a great signoff tool that allows the user to do many new things and debug timing like no other. Cadence is doing a great job with CTE and ETS and a good example of this is how quick are the big issues solved. After one year working with these tools, I can only say that they are a good alternative and a serious option for all sign-off engineers.

About the author

Alex was born in Oviedo (Spain) but lived the most time in Madrid. He started his career of Industrial Engineer in the Universidad Politecnica de Madrid (UPM). After the first 3 years of learning

the ground concepts of many fields (physics, maths, chemistry, thermodynamics, etc.), he decided to continue studies in the branch of electronics and to finish them in a German University (Technische Universitaet Darmstadt) with a double-diploma from both universities. This brought Alex the opportunity to learn the principles of the digital and analog designs and a first contact with the "industry" design tools like Virtuoso. His final project was the design of an Sigma-Delta Analog-Digital converter, designed in Virtuoso.

After his studies, Alex found a job in Freescale Semiconductor in Munich where he has now worked 2 years and a half working with highly experienced people and the most used tools in the market. Alex began to learn a lot of digital designs and how to set tools like SOC Encounter for almost all the phases in the backend-flow. Then took responsibility of the sign-off and delay calculation phases of Freescale designs in Munich, although he has done other tasks like CTS or extraction. Since working for Freescale, Alex has done many tapeouts in different technologies and used many different tools to achieve them.