DATASHEET

VOLTAGESTORM POWER AND POWER RAIL VERIFICATION

The complexities associated with today's power-sensitive designs increases the risk that IR drop will be a cause of silicon failure. Design teams require comprehensive power and power rail analysis solutions that can accurately validate on-chip power delivery networks, from initial power planning through final signoff prior to tapeout. Within the Cadence® Encounter® digital IC design platform, VoltageStorm® power verification helps you quickly validate and optimize your power networks using both static and dynamic analysis approaches.

ENCOUNTER PLATFORM

To release innovative products in narrow market windows, companies need to focus precious engineering resources on where they add the most value—differentiating their designs. The Cadence® Encounter® digital IC design platform offers a full spectrum of technologies for nanometer-scale SoC design, helping both logic design www.cadence.com/solutions/logic_design/index.aspx and physical implementation www.cadence.com/solutions/digital_implementation/index.aspx teams achieve high-quality silicon quickly. As an integrated RTL-to-GDSII design environment, the Encounter platform provides a complete flow—from RTL synthesis and test design through silicon virtual prototyping and partitioning to final timing and manufacturing closure. It delivers the highest quality of silicon (timing, area, and power with wires), accurate verification, signal-integrity—aware routing, and the latest yield and low-power design capabilities that are critical for advanced 65nm designs. With Encounter technology, you can boost your productivity, manage complexity, and get your products to market faster. Encounter platform products are available in L, XL, and GXL offerings.

VOLTAGESTORM POWER AND POWER RAIL VERIFICATION

Delivering the accuracy, capacity, and performance to handle the most complex multi-million gate designs, the VoltageStorm hierarchical solution gives design teams the confidence that IR (voltage) drop and power rail electromigration are managed effectively. VoltageStorm power verification has been proven to validate IR drop and power electromigration (EM) on thousands of designs. Initially used as an IR drop and power EM signoff solution prior to tapeout, VoltageStorm technology has evolved to become an integral component of design creation, which requires early and up-front power rail analysis to help create robust power networks during power planning. Employing parasitic extraction that is manufacturing aware, and using patented static and dynamic algorithms, VoltageStorm technology continues to deliver power estimation and power rail analysis functionality and automation that you can depend on to both analyze and optimize your power networks throughout the design flow.

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BENEFITS

- Enables efficient creation of on-chip power networks
  - Power routing sizes
  - De-coupling capacitance size and location
- Minimizes risk of power-related silicon failures
  - Outputs comprehensive static and dynamic IR drop reports
  - Enables IR drop-aware timing and SI noise analysis (requires Cadence Encounter Timing System or CeltIC® NDC)
- Optimizes low-power designs
  - Reports on-chip power density
  - Allows tradeoff between de-coupling capacitance and leakage
  - Validates power-switch sizes and power-up time
  - Verifies impact of power-up rush current on surrounding logic
- Delivers an efficient, hierarchical analysis solution
  - Uses power grid views to maximize accuracy, performance, and capacity
  - Accurately models IP, custom digital, analog, and mixed-signal blocks
- Supported by major reference flows, ASIC and IP vendors, and IDMs
  - Recommended by TSMC 7.0 Reference Flow
  - Recommended by Starc ZD 3.0 Flow
  - Library power grid views available directly from ARM and TSMC

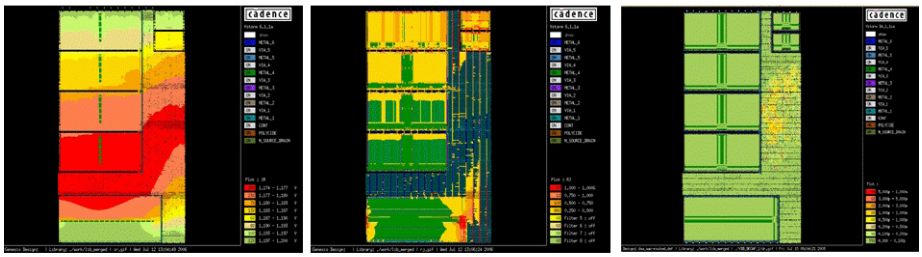

Figure 1: Example VoltageStorm plots (from left to right: IR drop, current density, and recommended de-coupling capacitance)

FEATURES

VoltageStorm power and power rail verification provides a comprehensive solution for power analysis and contains the functionality to accurately address the requirements associated with multiple design styles, including SoC, low-power, ASIC, and custom digital designs.

Employing a combination of static and dynamic analysis approaches, VoltageStorm solutions can be used for power rail verification during the complete physical design creation flow, from early power planning through signoff prior to tapeout. To enable this comprehensive support, the VoltageStorm solution contains the functionality to calculate static and dynamic power consumption plus the functionality to perform both static and dynamic power rail analysis.

POWER-DRIVEN DESIGN REQUIREMENTS

For design teams to manage power consumption effectively, they must understand the source of the power, typically either active power or leakage power. For design teams to create robust power networks, in addition to understanding the details of power consumption, they must understand how to optimize power rail routing and sizes and the size and location of power switches (low-power designs) and de-coupling capacitors. VoltageStorm technology contains all of the functionality required to help you with these power-driven design requirements.

POWERMETER POWER ESTIMATION

PowerMeter is the power estimation functionality within the hierarchical, cell-based VoltageStorm solution. PowerMeter allows you to calculate static power consumption and dynamic power

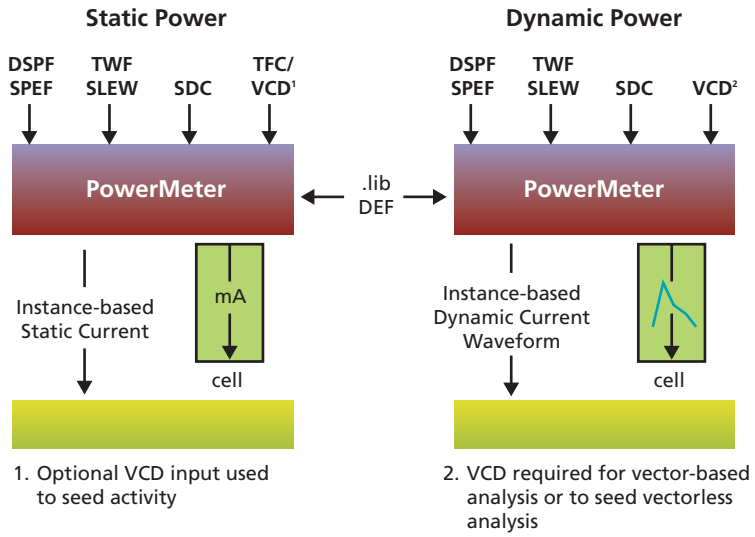

Figure 2: PowerMeter data flow and usage

transients for all instances within a design. Optional VCD vectors can be used to seed the activity for static or vectorless dynamic power calculation. VCD vectors can also be used to directly drive PowerMeter for vector-based dynamic power calculation.

PowerMeter uses a proprietary activity propagation algorithm that enables comprehensive nodal activity to always be generated, driven by default activity or seeded by partial activity information supplied by the designer.

VOLTAGESTORM PE

VoltageStorm PE enables hierarchical static power estimation using PowerMeter and hierarchical static power rail analysis.

A static approach to power rail verification helps you rapidly check that the power rails can supply the amount of power needed by the design, without creating high amounts of IR drop. Static analysis if often used for pre-tapeout signoff for process technologies at and above 130nm, where the amount of natural de-coupling capacitance diminishes the need for dynamic analysis.

Static analysis is a necessary step prior to executing dynamic analysis, to ensure that the power rails are robust prior to fine-tuning with de-coupling capacitance—incorrectly sized power routing cannot be fixed by adding de-coupling capacitance.

VOLTAGESTORM DG

With hierarchical vectorless and vector-based dynamic analysis, VoltageStorm DG extends the static analysis capabilities of VoltageStorm PE.

At and below 90nm, high dynamic currents caused by simultaneously switching logic can cause high transients of dynamic IR drop on both power and ground rails. Using VoltageStorm DG, design teams can determine the dynamic power consumption created by simultaneous switching and the dynamic IR drop caused by these high currents.

Both VoltageStorm PE and DG provide full support for low-power design methodologies that employ multiple voltage domains, multiple thresholds,

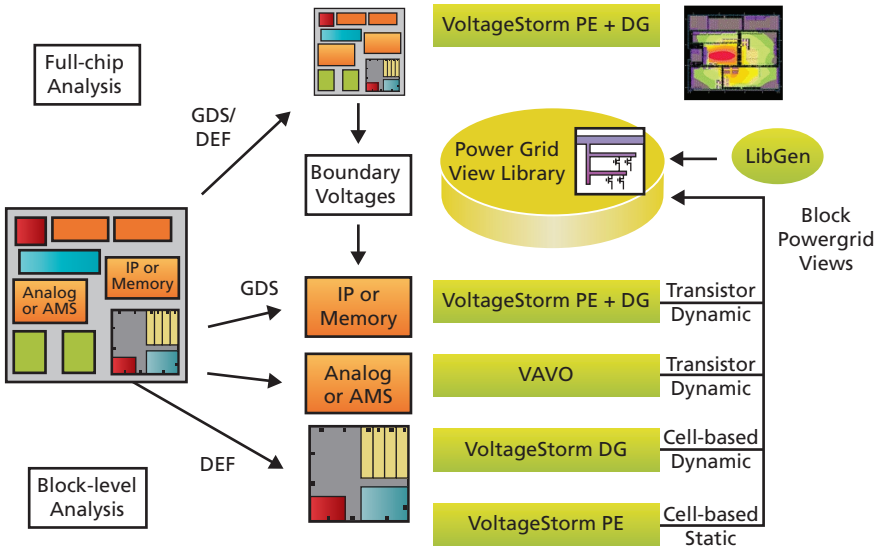

Figure 3: Hierarchical power rail analysis

level-shifting logic, voltage clamp circuitry, and the use of power switches to minimize leakage. VoltageStorm DG gives you additional insight on how fast a block powers up after it was powered down, and the IR drop impact of the block powering up on surrounding logic.

TRANSISTOR-LEVEL ANALYSIS

With the VoltageStorm hierarchical analysis solution, you can use the technology at the transistor-level to perform power rail analysis for custom digital blocks. Using GDSII input and the Virtuoso® UltraSim simulation engine, the VoltageStorm solution enables static- and vector-based dynamic analysis.

AUTOMATED DE-COUPLING CAPACITANCE OPTIMIZATION

Once you've completed dynamic power rail analysis using VoltageStorm DG, the solution can calculate and recommend the amount of additional de-coupling capacitance necessary to limit the dynamic IR to user-specified limits. This recommended additional de-coupling capacitance can then drive an automated optimization flow within the SoC Encounter™ system, where filler cells are swapped with de-coupling capacitance cells.

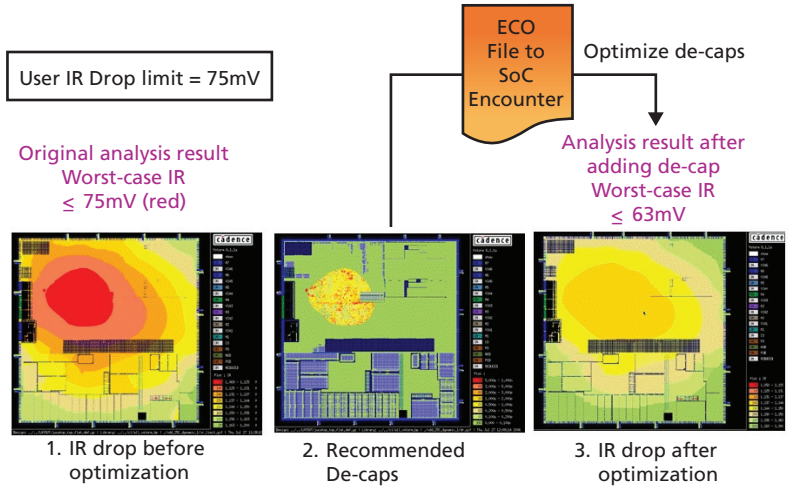

Figure 4: Automated de-coupling capacitance optimization flow

IMPACT OF IR DROP ON TIMING AND SI NOISE

While some design teams use IR drop margins to ensure that their designs will not suffer from IR drop issues, a more comprehensive approach is to fix IR drop issues that are shown to impact timing and SI noise.

VoltageStorm technology calculates instance operating voltages during the timing (switching) windows associated with each instance, and provides this information to Encounter Timing System or CeltIC NDC, which calculate the impact of IR drop on delay- and SI-generated noise.

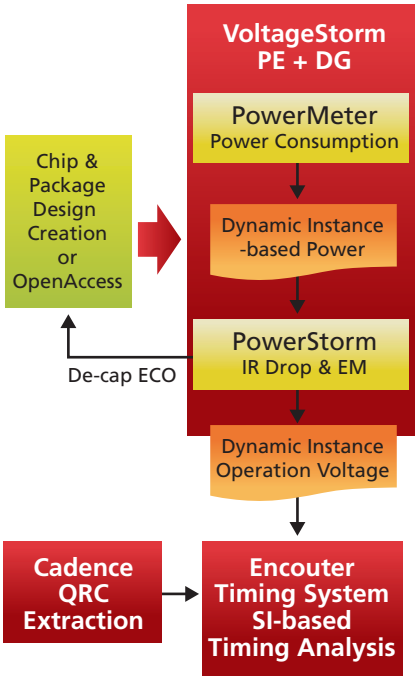

Figure 5: Flow to analyze impact of IR drop on timing and SI noise

SPECIFICATIONS

SYSTEM REQUIREMENTS

Specific requirements are design dependent

- 512MB (min) DRAM
- 2GB (min) swap space
- 50MB software disc space
- 2GB per 1M gates design disc space

PLATFORM/OS

- Sun Solaris 8 or 9 (32-bit, 64-bit)
- HP-UX 11.0 (32-bit, 64-bit)
- Opteron Linux RHEL 3.0 (64-bit)
- Red Hat Linux RHEL 2.1 (32-bit)
- BM AIX 5.1 (32-bit, 64-bit)

INTERFACE

- OpenAccess 2.2

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