cadence®

Cadence Virtuoso Digital Implementation

Timing-driven digital block implementation for a mixed-signal design methodology

Cadence® Virtuoso® Digital Implementation is a complete and automatic system for RTL-to-GDSII block implementation. Based on Encounter® RTL Compiler and Encounter Digital Implementation System core technology with superb performance and accuracy in synthesis, implementation, and optimization, the system enables capacity-limited timing-driven block physical implementation from gate-level synthesis with design for test, to floorplanning, placement, routing, and optimization, in the context of an advanced analog-driven mixed-signal design.

Reach Fast Design Closure on All Objectives

As a part of Cadence's interoperable mixed-signal methodology on OpenAccess common database, Virtuoso Digital Implementation automatically ensures digital blocks are implemented per timing, power, signal integrity (SI), and physical specifications correctly and consistently across digital and analog boundaries, and across multiple power domains at all time. This implementation allows customers to reach a fast design closure on all objectives for complex mixed-signal designs.

Benefits

- Rapid design closure and shorter overall design cycle
  - Timing-driven implementation uses a common (Encounter) timing engine and a signoff-quality delay calculator
- Faster convergence on design goals and fewer iterations
  - Concurrent design and optimization of timing, area, and power minimizes and eliminates late-stage unwanted surprises

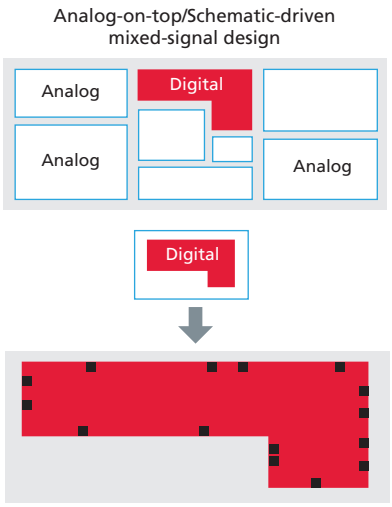

Figure 1: Virtuoso Digital Implementation for smaller digital block implementation in a mixed-signal design

- Unified design intent and abstraction through integration with the Virtuoso platform ensures consistent design constraints throughout the entire flow
- Co-design of digital and analog components in a single environment
  - Built-in OpenAccess interoperability enables fast and precise top-level integration
- Rapid timing convergence for mixed-signal blocks
  - Ensures accurate static timing analysis of all digital logic paths using full-timing models and physical optimization
- Integrated power planning, power routing, and what-if power analysis enables smart power rail synthesis
- Support for multiple power domains enables a low-power methodology
- State-of-the-art clock tree synthesis
  - Optimizes clock gating for low-power designs; supports multiple and re-convergent clocks

Features

RTL synthesis

- Physical- and power-aware synthesis
- Read/write standard inputs/outputs
- Built-in high-performance data path
- Arithmetic optimizations
- Total negative slack (TNS) optimization
- Testability analysis and scan insertion
- Clock gating

- Multi-volt leakage power optimization
- RTL synthesis with low power

Design exploration and prototyping

- EDI System floorplanning prototyping capability for early feasibility
- Timing-driven fast standard cell placement
- Built-in consistent parasitic extraction for timing and power analysis
- Advanced delay calculation for timing analysis using industry-standard timing library and constraints formats
- Multi-objective state-of-the-art optimization technology with GigaOpt for best overall quality of results (QoR)
- In-place optimization for cell resizing, buffer insertion, and load splitting
  - Leakage power optimization
  - Advanced logic restructuring option

Clock tree synthesis

- Automatic physical and power-aware clock tree synthesis to minimize clock skew, insertion delay, and area
- Support for gated clocks and multiple clock domains
- Post-route clock tree optimization
- Useful skew analysis and optimization

Advanced power planning

- Automation for accurate planning for power distribution and power switch insertion
- Built-in power/IR drop analysis and interface to signoff power-grid verification*
- Power-grid design results in IR drop numbers within 10% of SPICE
- Guided clock trunk/branch routing by NanoRoute

Placement and routing

- LEF/DEF data transfer via standard interfaces and OpenAccess
- Rectilinear block support
- Industry-proven advanced NanoRoute technology with timing, area, SI, and DFM awareness
- Support for advanced engineering change order (ECO) routing
- Wire editor capability over signal and power
- CPF-driven automatic low-power design including multi-supply voltage in power shutoff, DVFS support, and more
- SI and MMMC support

Easy to use

- Tcl programming interface throughout the flow
- Intuitive and helpful commands
- Link to Virtuoso Space router for special mixed-signal nets
- Block implementation foundation flow to ramp-up design methodology within a week
- Debugging capability and helpful reports for all steps

Specifications

Input

- HDL (to synthesis): Verilog, VHDL, SystemVerilog (directives, pragmas)
- Logical and timing library: library format (.alf), TLF, .lib
- Physical library: LEF
- Mixed-language/mixed-level netlist: gate-level netlist in Verilog, gate-level EDIF netlist
- Timing constraints: SDC
- Floorplan information: PDEF
- Detailed floorplan information: DEF
- Delay information: SDF
- Interconnect parasitics: DSPF/RSPF, SPE

Output

- Optimized gate-level netlist (from synthesis)
- Netlist: DEF, Verilog
- Interconnect parasitics: DSPF, SPICE, SPEF
- Delay information: SDF
- Floorplan and placement: DEF, PDEF
- GDSII

Platforms

- Linux (32- and 64-bit)
- Solaris (64-bit)
- SOLX86 (64-bit)
- IBM AIX (64-bit)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, and software downloads, and more.

* Interface to signoff power-grid verification requires an Encounter Power System license, which must be purchased separately

cadence®

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud and connectivity applications. www.cadence.com

951 07/13 SA/DM/PDF