Fast and Accurate Statistical Cell Characterization using Spectre

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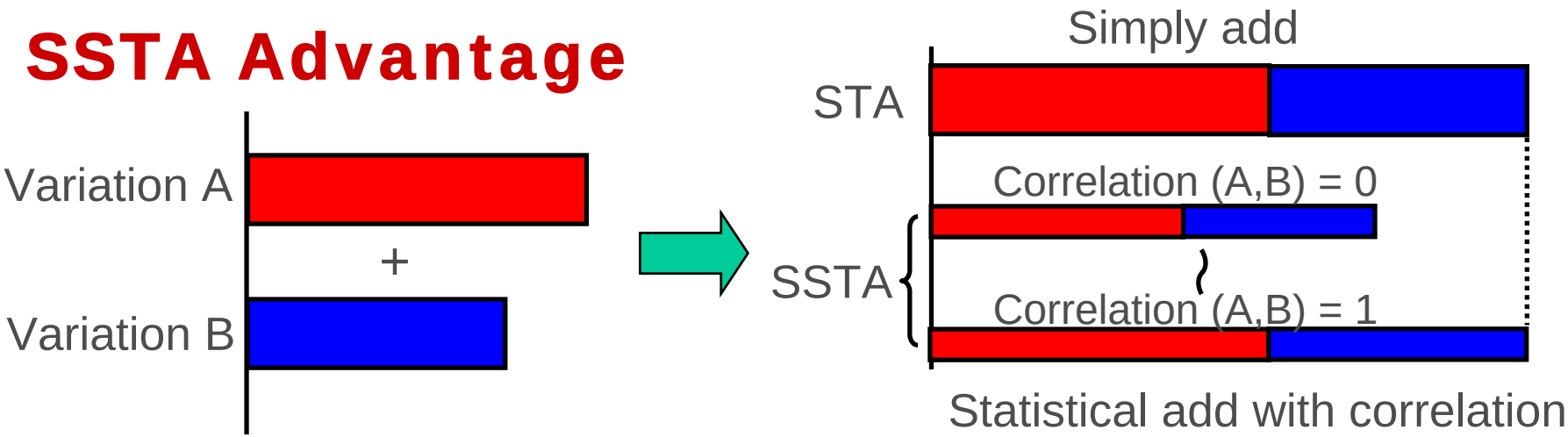
Agenda

- Introduction
- Cell characterization overview
- Process variation modeling
- Statistical cell characterization
- Benchmark Results
- Conclusion

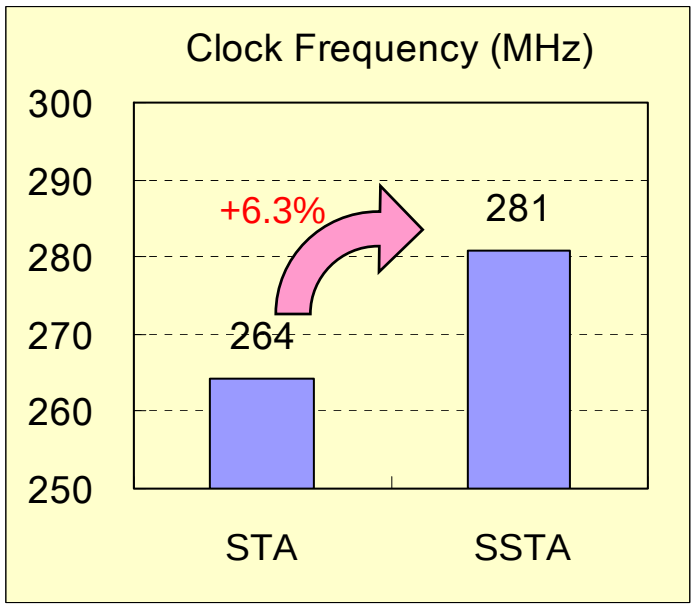
Introduction

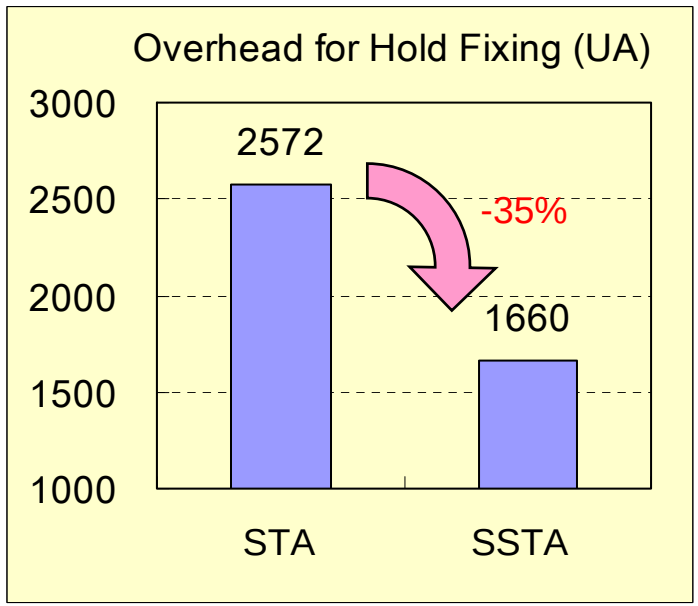
- Statistical static timing analysis (SSTA) offers a number of advantages over traditional corner based static timing analysis.
  - SSTA provides a more realistic estimation of timing relative to actual silicon performance.
  - Enables designers to optimize timing paths with biggest impact on overall performance, rather than paths that may fail only at extreme corners.
- Statistical cell model is a key enabler for SSTA.

SSTA Advantage



SSTA removes statistical pessimism of STA.





Circuit : DSP core block
w/o scan test circuit
Area : 570um x 570um
Gate : 340kUA

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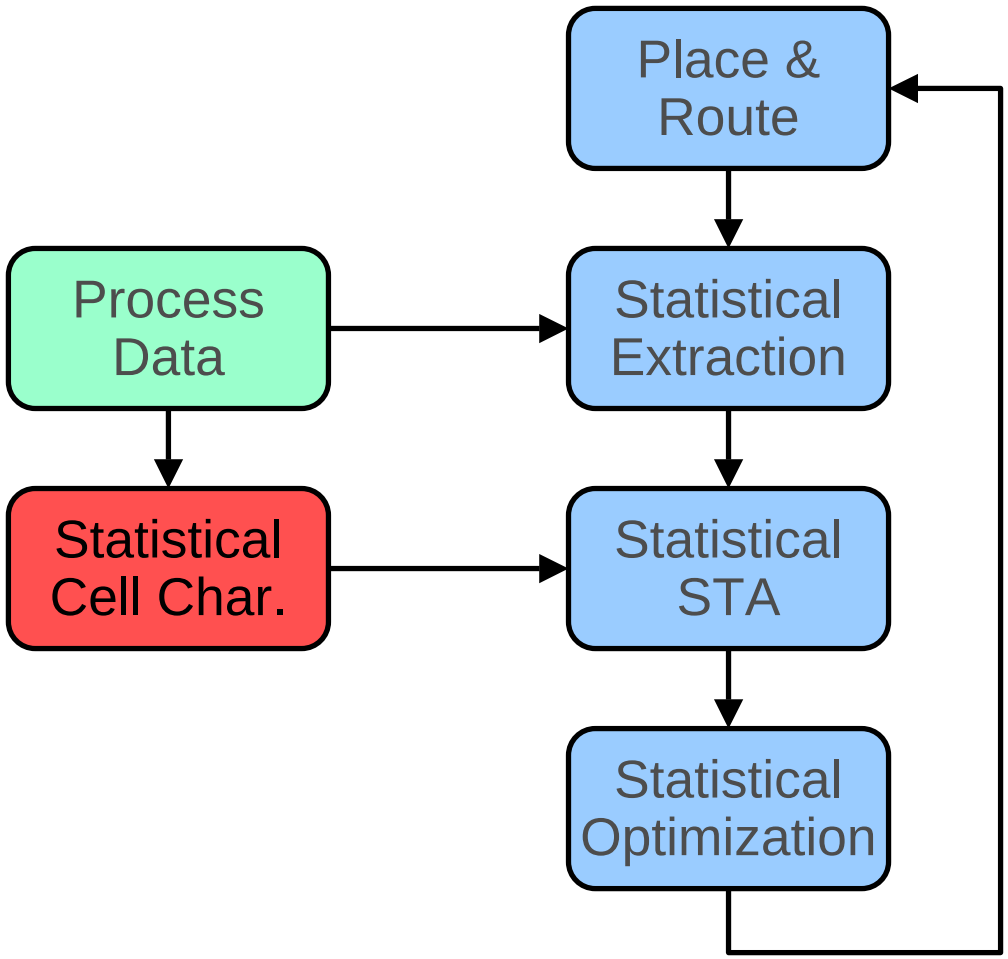
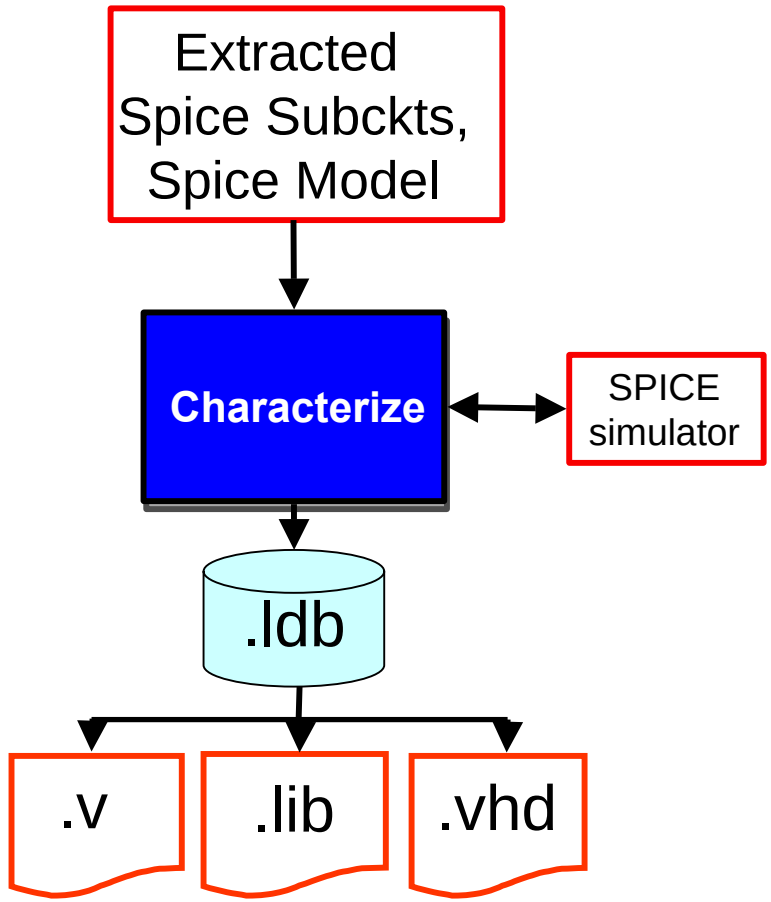
Statistical Design Flow



Regular Cell Characterization

- Extract electrical behavior from Spice netlist & models.
- Requires millions of Spice simulations over a compute farm.
- Outputs lookup tables for optimization & signoff tools.
- Usually takes weeks to complete.

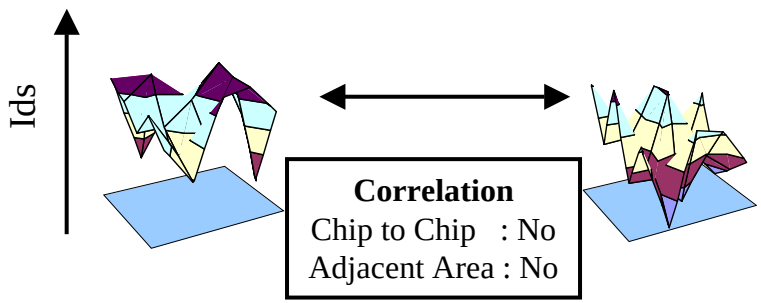


From Regular Library to Statistical Library

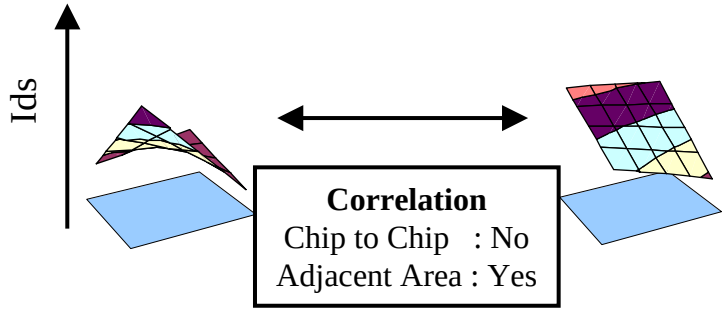
- Process Variation Models
- Throughput requirement
  - Base characterization system must speed up by 10x to handle large increase in Spice simulations.
- Consistency in characterization conditions
  - Input waveform
  - Measurement methods, e.g. pin cap, setup/hold
  - State dependencies
  - Table indices
  - NLDM vs. current based model
  - Spice simulation settings

Process Variation

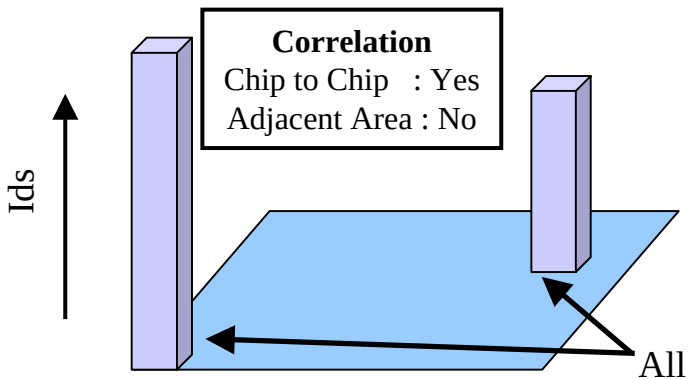
[Random] On Chip Random



[Systematic] On Chip Systematic

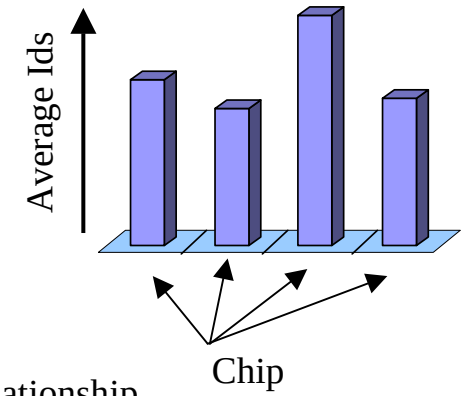


[Deterministic] On Chip Deterministic



All chips have same relationship

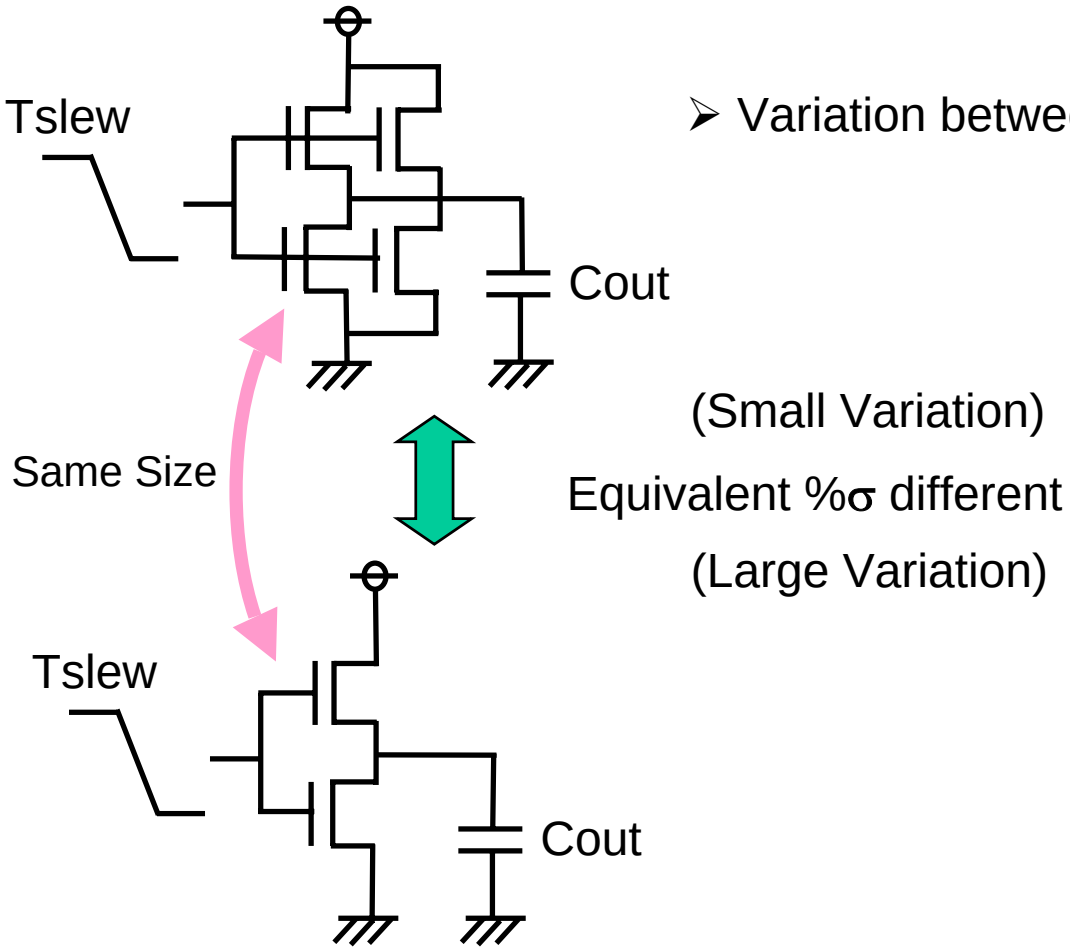
[Global] Off Chip Systematic



Average difference between chips

“Random” Variation (Intra-Cell)

Random variation has no correlation among transistors inside circuit



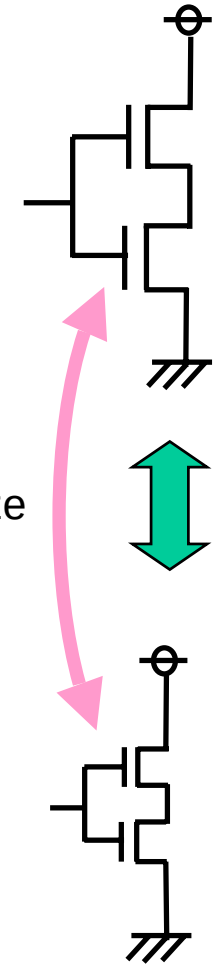
- Variation between transistors is independent.

(Small Variation)

Equivalent %σ different

(Large Variation)

“Random” Variation (Pelgrom effect)



Same #
Different Size

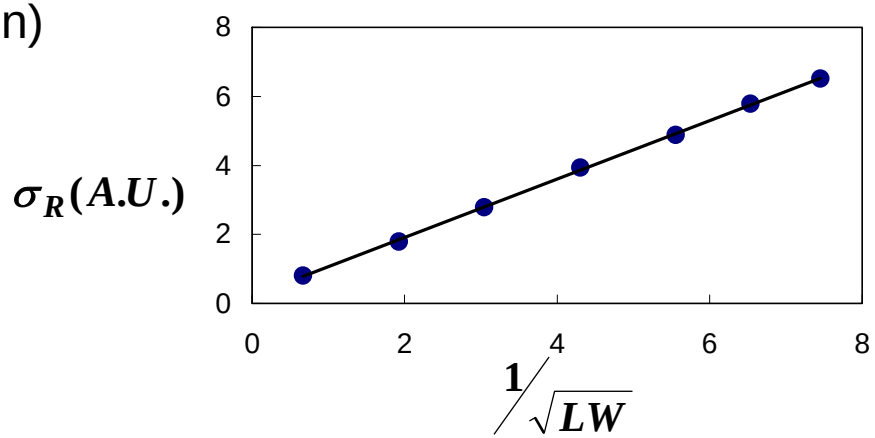
(Small Variation)

Equivalent %σ different

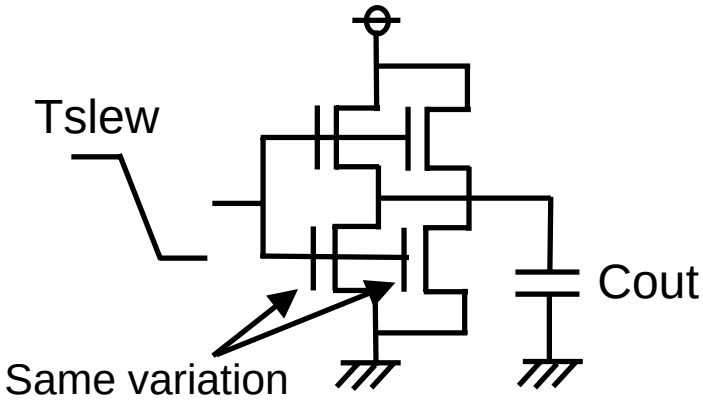
(Large Variation)

- Variation of each transistor depends on the size
  Pelgrom pointed out variation depends on $\frac{1}{\sqrt{LW}}$ so called Pelgrom effect

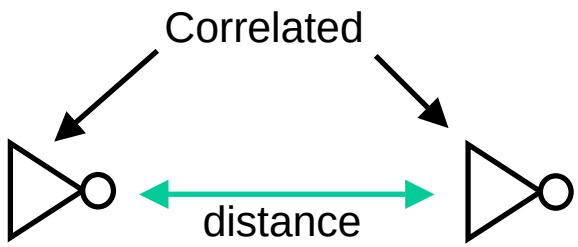
Renesas 90nm Process Measurement Data with various L and W of transistor



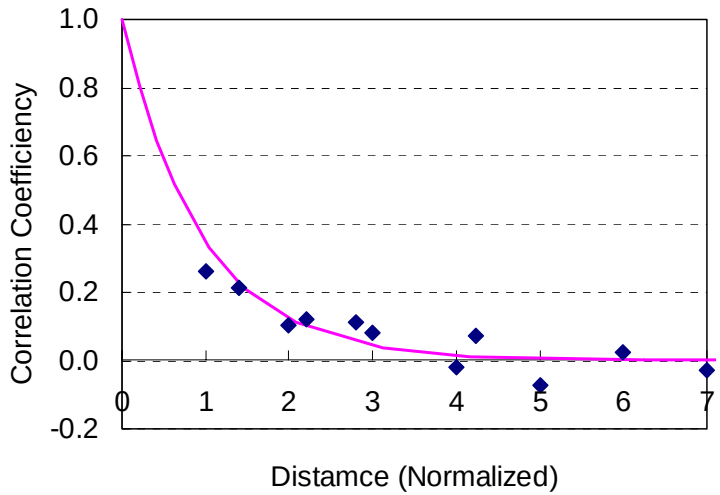
“Systematic” Variation (Distance-based)



- Variation between transistors inside cell is same.
- Correlation between cells are function of distance



Renesas 90nm Process Measurement Data of Systematic (Distance Base)



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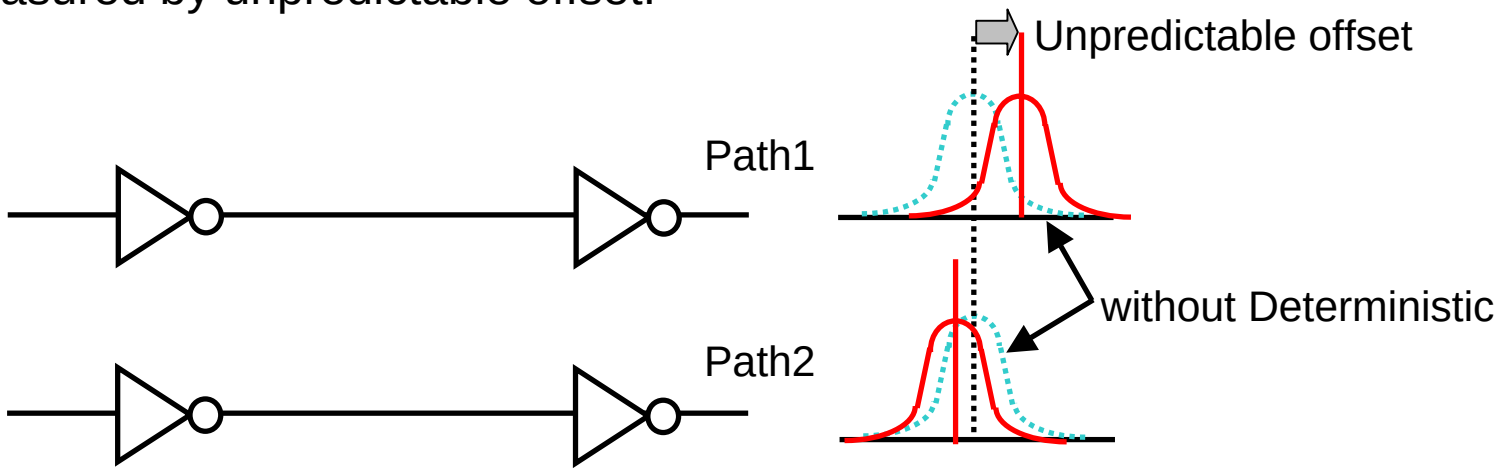
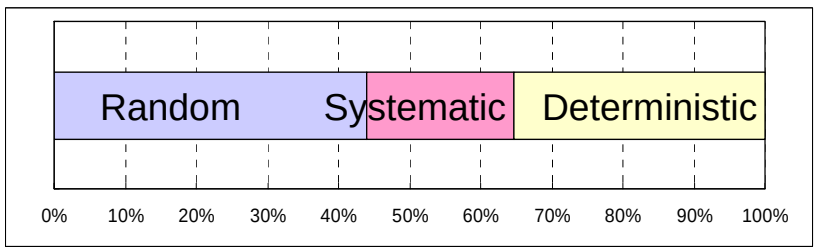
“Deterministic” Variation

Deterministic variation is NOT statistical variation,
but need to be considered like guard band in SSTA to avoid yield down.
Deterministic variation is well correlated between chips (coefficiency = 1)
and measured by unpredictable offset.

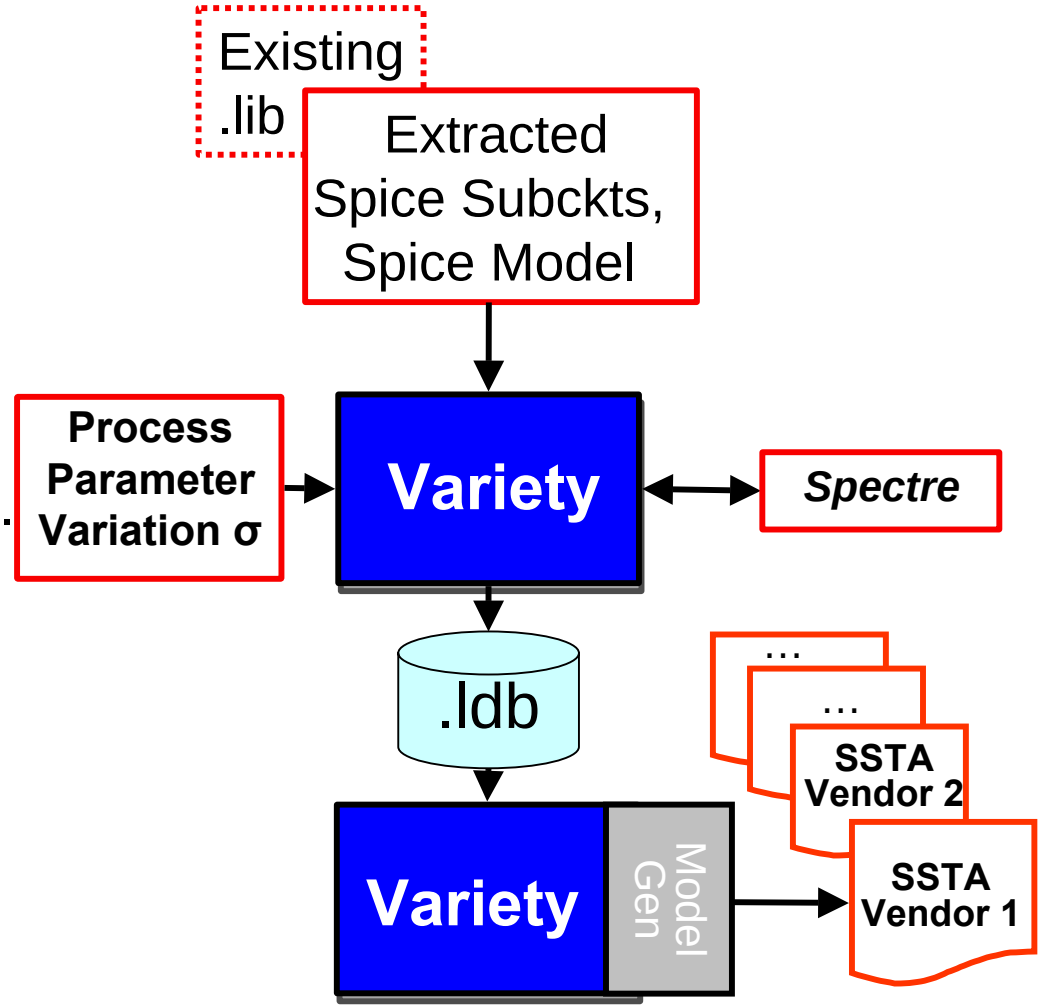


90nm On Chip variation contribution with 7 stages inverter chain



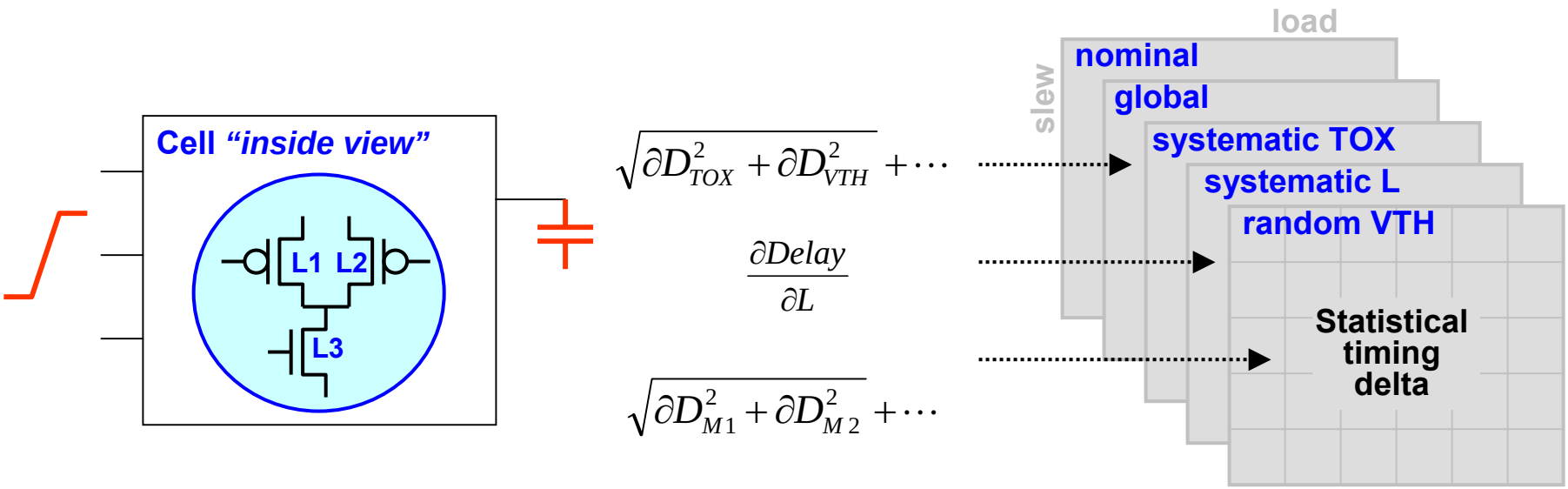
Statistical Cell Characterization

- Compare to regular cell characterization, additional input is process parameter variation and correlation.
- Model process variation's impact on delay, constraints (setup, hold etc.), pin capacitance, power, leakage.
- Outputs multiple SSTA formats without re-characterization.
- Base characterization system must speed up by 10x to avoid SSTA characterization being bottleneck.



Statistical Cell Models

- **Systematic variation** – inter-cell variation
  - Process variation correlated between transistors
  - e.g. L varies by 5%, Tox varies by 3% for all transistors inside cell
- **Random variation** – intra-cell variation
  - Process variation uncorrelated between transistors
  - e.g. Vth variation inversely proportional to sqrt(L*W)



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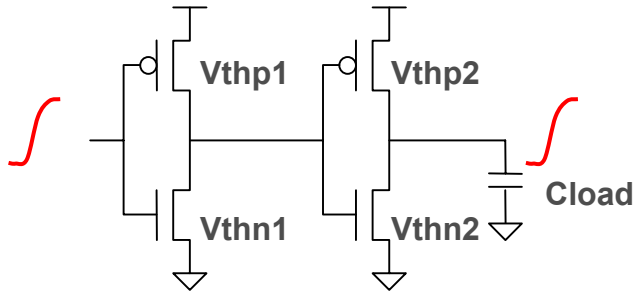
Random Variation Characterization

- Each transistor inside a cell has unique impact on delay, transition, pin capacitance and power.
- The total impact from each transistor must be captured as a standard deviation for each table entry.



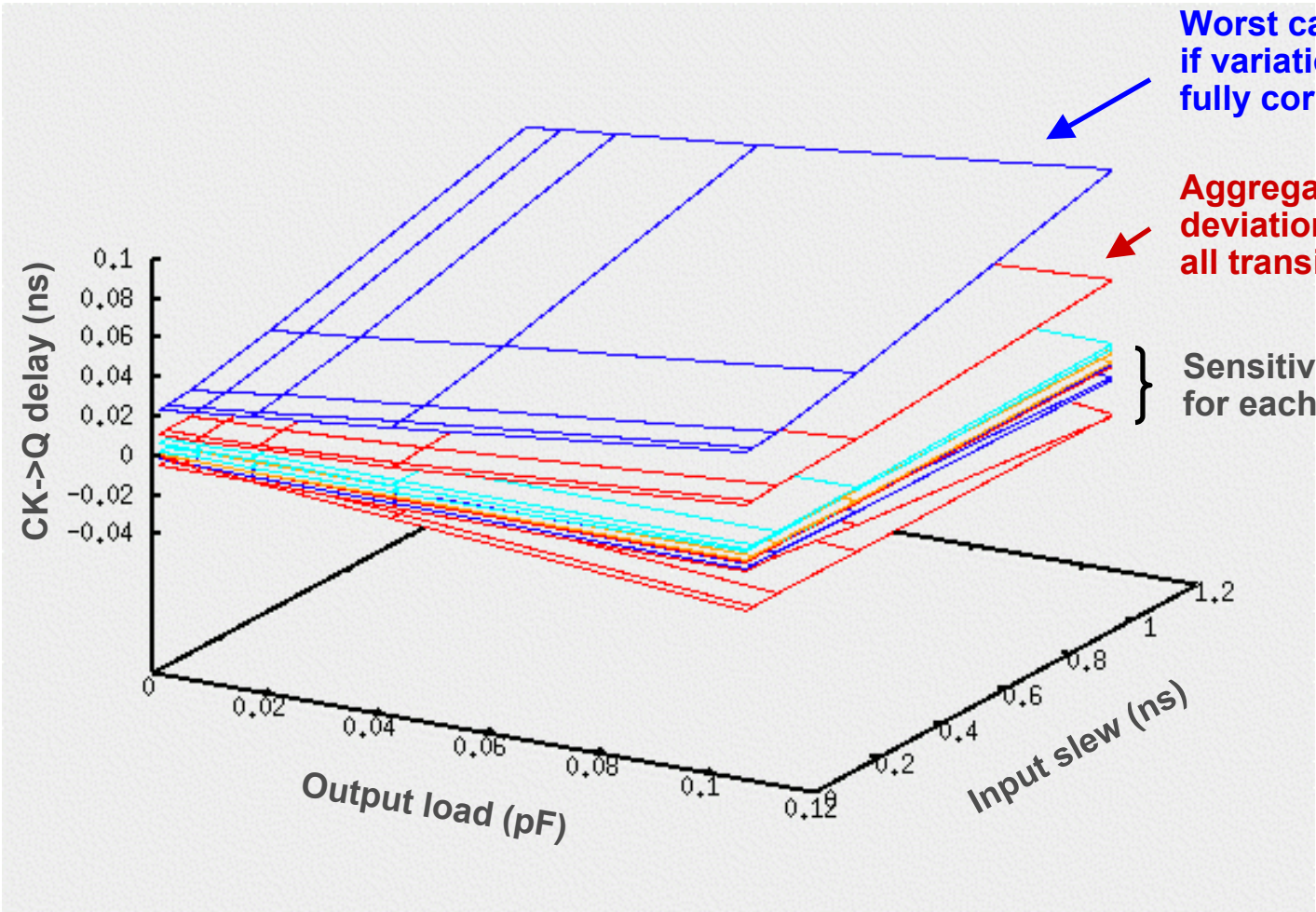
Simple buffer with random threshold voltage variation

Random threshold voltage variation for a buffer and its effect on rise delay and pin capacitance

	Nominal	d(Vthn1)	d(Vthp1)	d(Vthn2)	d(Vthp2)	sigma
Delay(Cload=16fF)	97ps	7.3ps	0.04ps	0.24ps	3.6ps	8.1ps
Delay(Cload=64fF)	127ps	7.6ps	0.04ps	0.22ps	6.9ps	10.3ps
Input Pin Cap	3.3fF	0.07fF	0.04fF	0	0	0.08fF

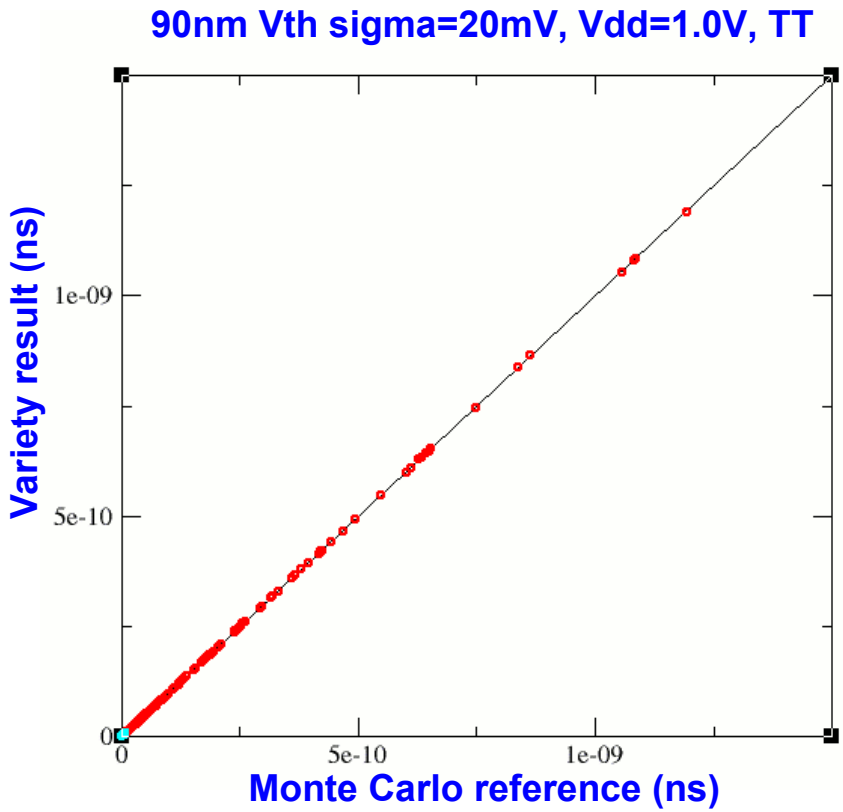
Random Variation NLDM Surfaces

Random delay variation for each of 24 transistors inside a DFF, CK->Q rise delay arc, and the standard deviation on their aggregate delay impact.



Model Accuracy

- Linear and non-linear models
  - ΔDelay(Vth+5%) != ΔDelay(Vth-5%)
  - Linear sensitivity or Non-linear CDFs
- Random variation
  - Analyzes each parameter's impact on each transistor and how it affects the arc delay.
  - Transistor sensitivity analysis to avoid runtime explosion.
  - Verified with Monte Carlo simulations
- Consistency between .lib and SSTA libraries

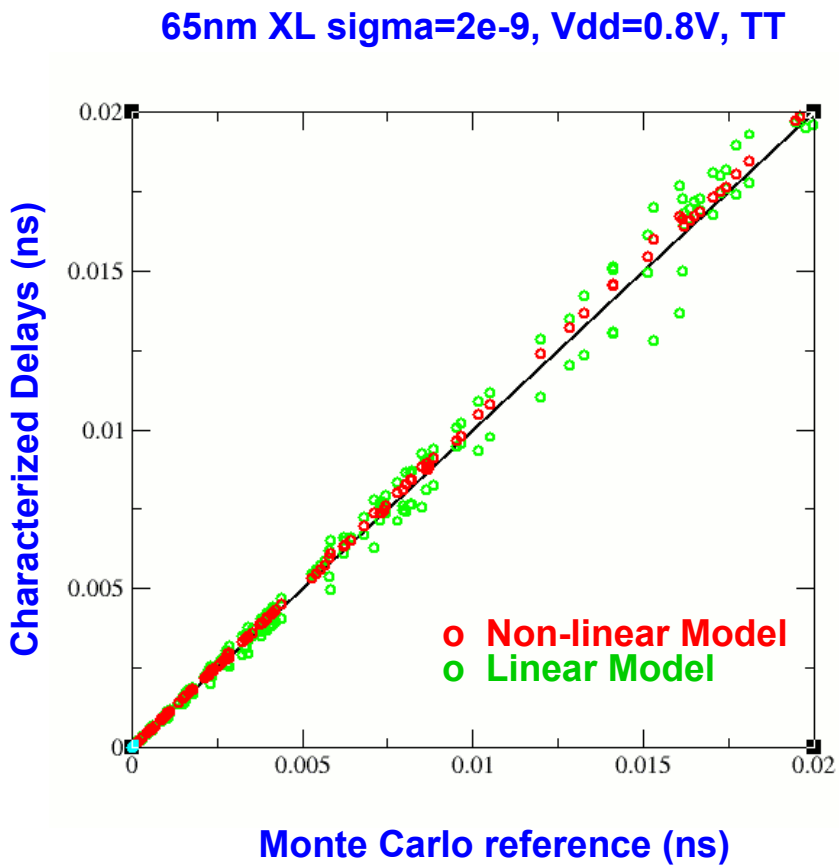


Library	CPUs	Variety Runtime*	Liberate Runtime
387 cells	8	6hrs	1hr

*1 random, 3 systematic parameters

Non-Linear Models

- The effect of process variation becomes more non-linear with geometry scaling and Vdd scaling
  - ΔDelay(L+5%) != ΔDelay(L-5%)
- Variety supports both linear and non-linear models
  - Linear variation expressed as delta or sensitivity
  - Non-linear variation can be modeled as cumulative distribution functions (CDF) using Altos Fast Monte Carlo method.



SSTA Characterization Example

```
# Define random threshold voltage variation
define_variation -type random -pelgrom {
      dvthn   5.1e-9
      dvthp   3.2e-9
} RANDOM_VARIATION

# Define systematic length & width variation that are 100% correlated
define_variation -type systematic {
      dxl       1.67e-9
      dxw       2.33e-9
} SYSTEMATIC_VARIATION

# Define systematic threshold voltage and oxide thickness variations
define_variation -type systematic {dvthn       0.04}      SYSTEMATIC_NVTH
define_variation -type systematic {dvthp       0.04}      SYSTEMATIC_PVTH
define_variation -type systematic {toxn       2.90e-9}    SYSTEMATIC_NTOX
define_variation -type systematic {toxp       3.07e-9}    SYSTEMATIC_PTOX

# Define global variation between 4 uncorrelated systematic parameters
define_variation_group {
   SYSTEMATIC_NVTH
   SYSTEMATIC_PVTH
   SYSTEMATIC_NTOX
   SYSTEMATIC_PTOX
} GLOBAL_VARIATION
```

SSTA Library Example

```
altos_variation (RANDOM_VARIATION) {
  param : "dvthn dvthp";
  pelgrom : true;
  sigma : "5.1e-09 3.2e-09";
  type : random;
}
altos_variation (SYSTEMATIC_VARIATION) {
  param : "dxl dxw";
  sigma : "1.67e-09 2.33e-09";
  type : systematic;
}
altos_variation (SYSTEMATIC_NVTH) {
  param : "dvthn";
  sigma : "0.04";
  type : systematic;
}
altos_variation (SYSTEMATIC_PVTH) {
  param : "dvthp";
  sigma : "0.04";
  type : systematic;
}
altos_variation (SYSTEMATIC_NTOX) {
  param : "toxn";
  sigma : "2.9e-09";
  type : systematic;
}
altos_variation (SYSTEMATIC_PTOX) {
  param : "toxp";
  sigma : "3.07e-09";
  type : systematic;
}
```

```
cell_rise (delay_template_3x3) {
    index_1 ("0.0126438 0.123177 1.2");
    index_2 ("0.000530155 0.0441719 0.11043");
    values ( \
      "0.246609 0.50421 0.88925", \
      "0.287316 0.544926 0.929964", \
      "0.494653 0.752258 1.13738", \
      "0.00987928 0.0152166 0.0289518", \
      "0.0109284 0.0159453 0.0293591", \
      "0.0323984 0.0345518 0.0426152", \
      "0.00313418 0.00647137 0.0114758", \
      "0.00331954 0.00667415 0.0116211", \
      "0.00631122 0.00965918 0.0146037", \
      "0.0164899 0.0167667 0.0167401", \
      "0.0166293 0.0169202 0.0168761", \
      "0.0119603 0.0122492 0.0122077", \
      "-0.0199854 -0.0495935 -0.0946429", \
      "-0.023522 -0.0531199 -0.0981904", \
      "-0.0696555 -0.0992671 -0.144338", \
      "0.000847658 0.00089532 0.000883976", \
      "0.000852426 0.000890052 0.000888674", \
      "0.000635933 0.000672701 0.000670396", \
      "-0.000840775 -0.00203027 -0.00378917", \
      "-0.00104065 -0.00222294 -0.00399243", \
      "-0.00380699 -0.0049865 -0.00676231" \
    );
  }
```

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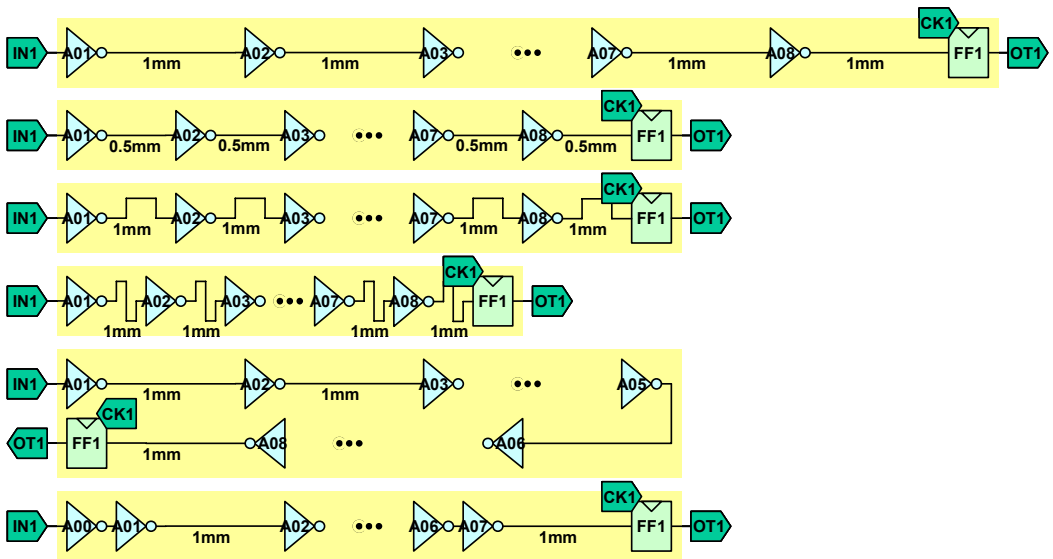
SSTA Benchmark

- 18 benchmark circuits (90nm) to test accuracy of statistical analysis flow, including statistical cell library and statistical timing analyzer.
- Compare “mean” with Spectre simulation.
- Compare “sigma” with Spectre Monte Carlo simulation with 2000 trials.

Benchmark Circuits

- 7 inverter circuits
  - Inverter chains 1, 8, 16 and 64 deep.
  - x0.5, x1, x4 drive strengths.
  - Fanouts of 1 and 4.
- NAND2, NOR2, AO22, XOR2, BUF
- 6 circuits with long interconnects and placement variations.



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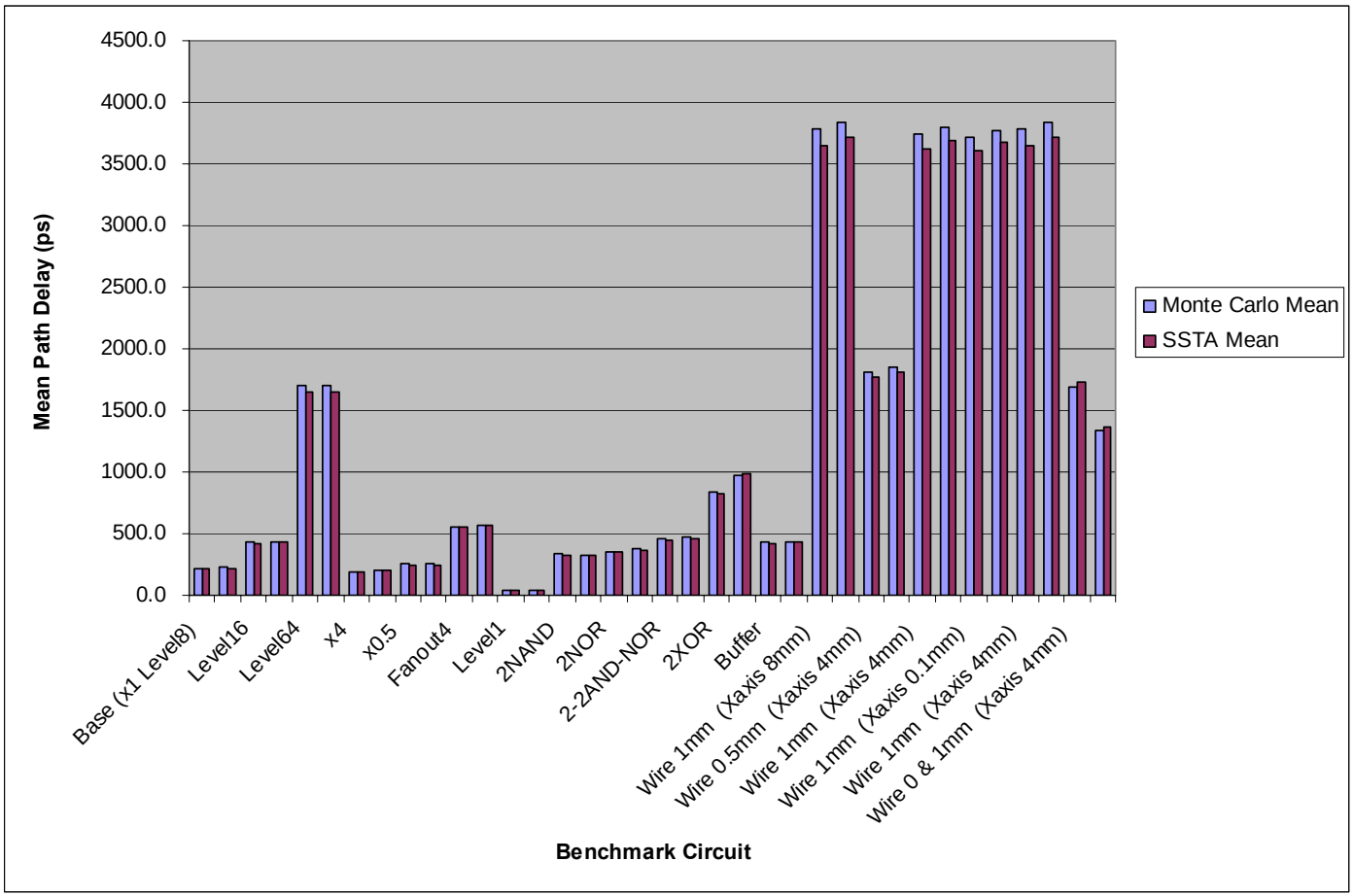
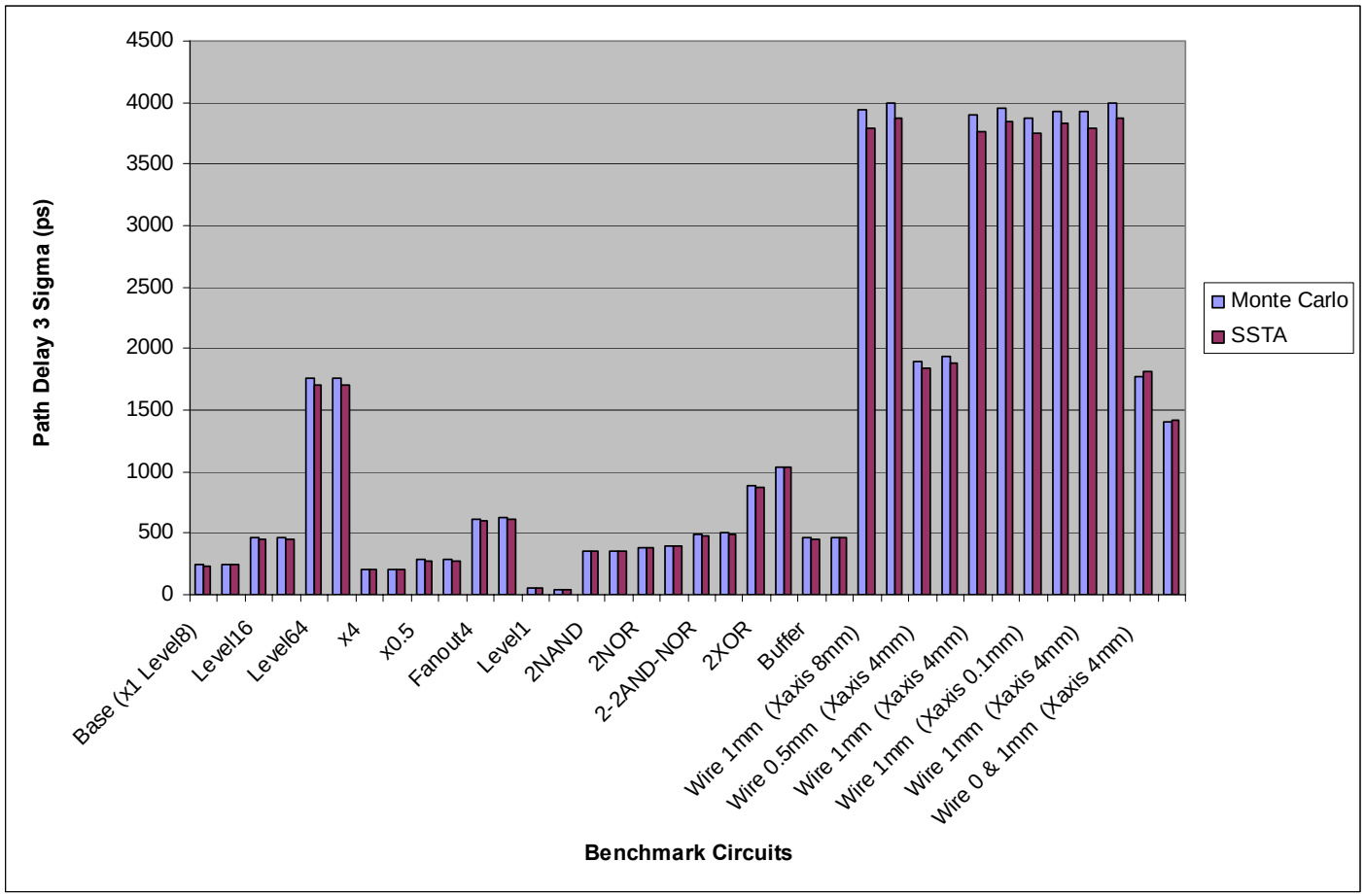
Mean Path Delay Results



Random Variation Path Delay Results

Vth0, XL



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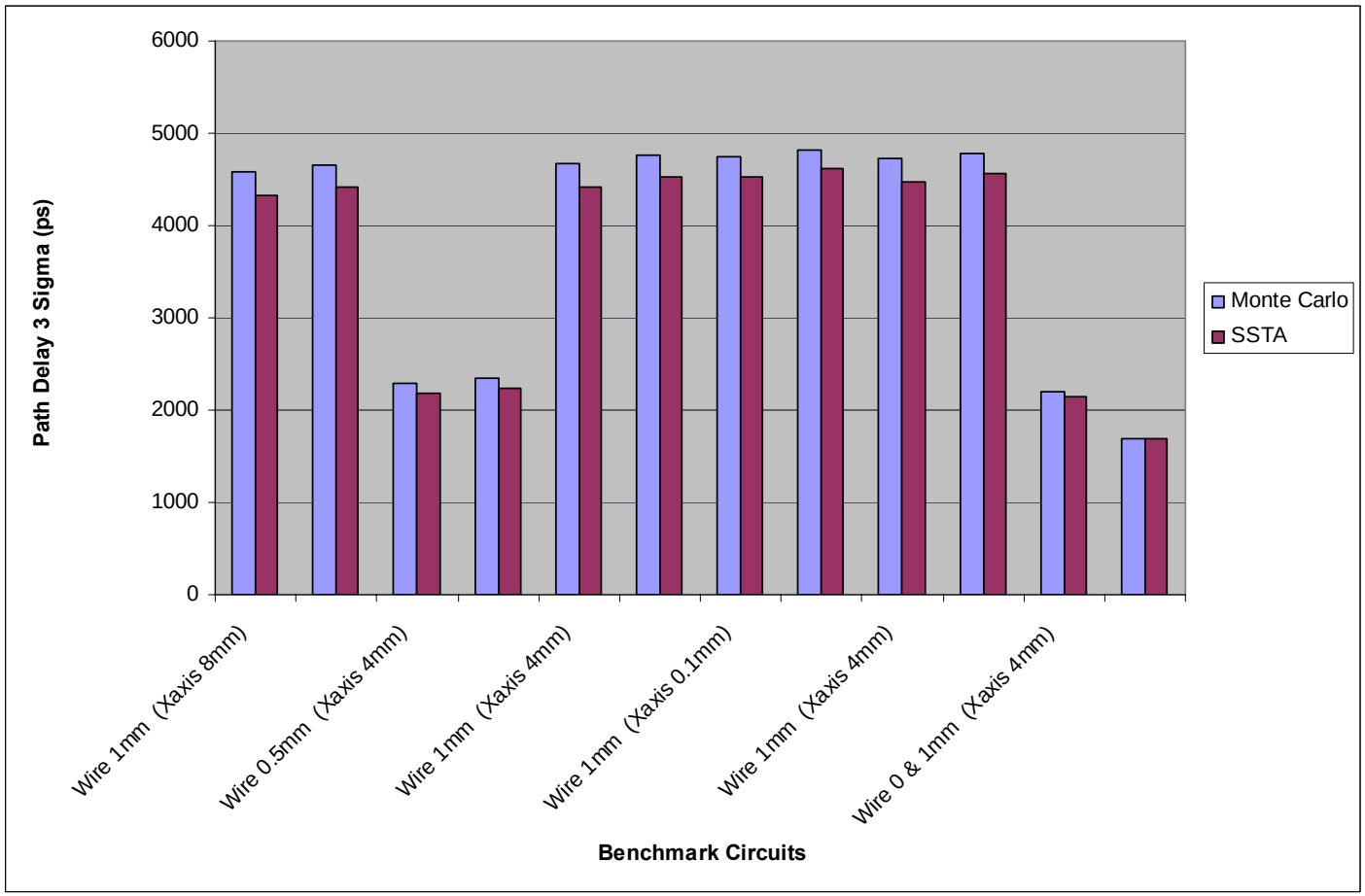
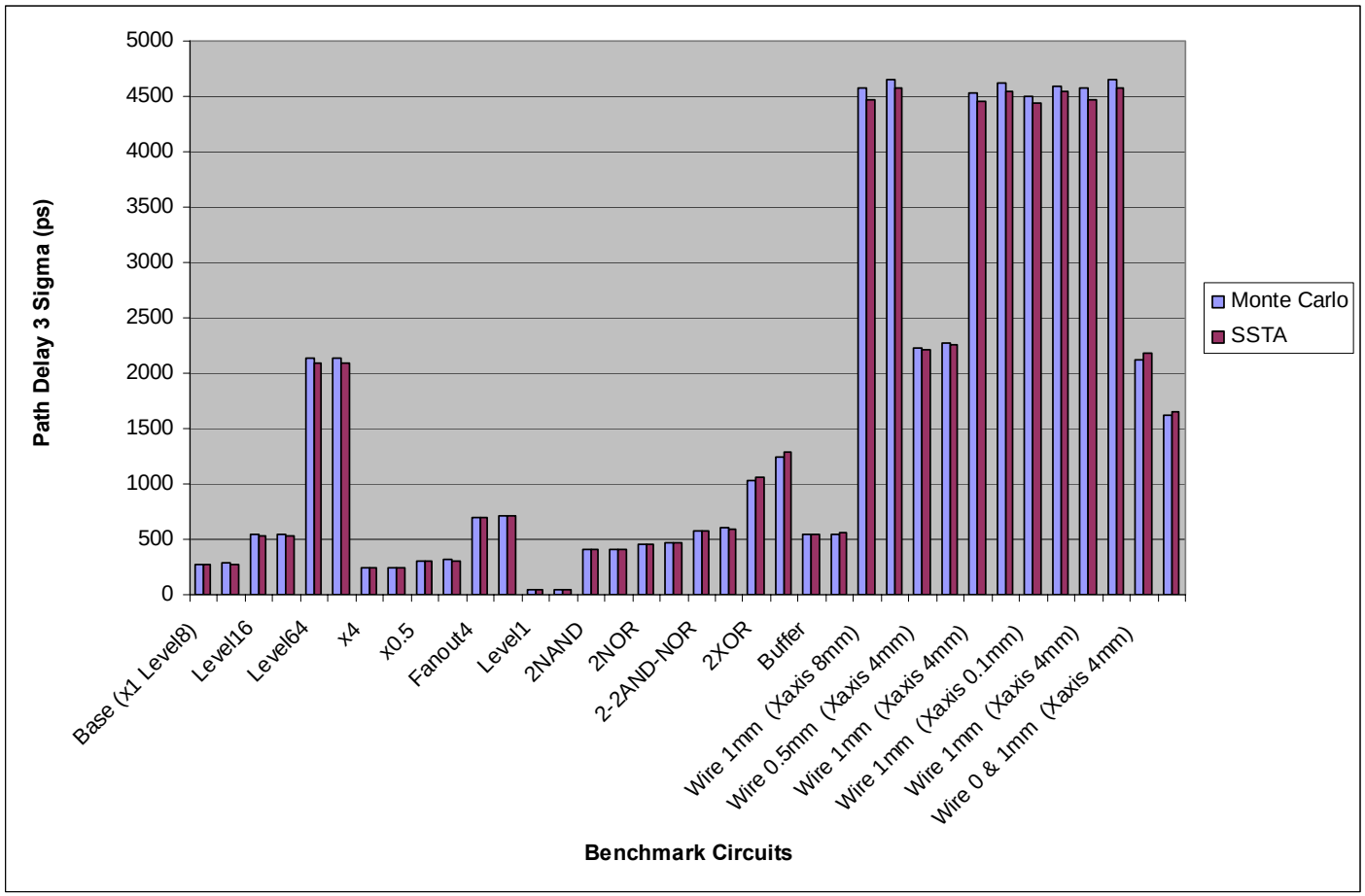
Systematic Variation Path Delay Results

Vth0



Global Variation Path Delay Results

Vth0, XL



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Benchmark Summary

	Mean	Mean + Random 3σ	Mean + Systematic 3σ	Mean + Global 3σ
Avg Diff	-1.5%	-1.8%	-4.2%	-0.4%
Std Dev	1.6%	1.6%	1.7%	1.6%

Conclusion

- A practical characterization system providing consistency between corner-based library and the new requirements of SSTA library has been described.
- SSTA accuracy has been validated with Monte Carlo simulations on benchmark circuits.
- Legacy characterization systems must be overhauled to handle the throughput and flexibility requirements of SSTA characterization.