cadence®

Cadence DFM Services

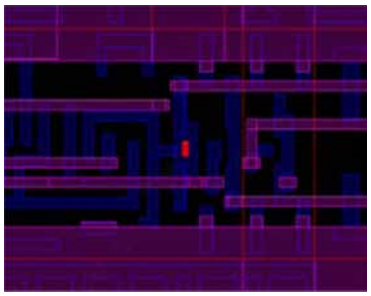
Simulation, hotspot detection/correction, and verification down to 28nm

Cadence® DFM® Services is a turnkey offering that provides customers with optimal time to productivity. It combines industry-leading, production-proven technology and tools, methodologies, services, collaboration, and IT infrastructure. Cadence DFM Services leverages knowledge from across the Cadence engineering, foundry, and applications teams. The result is a robust, timely service that enables customers to complete signoff litho and CMP analyses on advanced node designs.

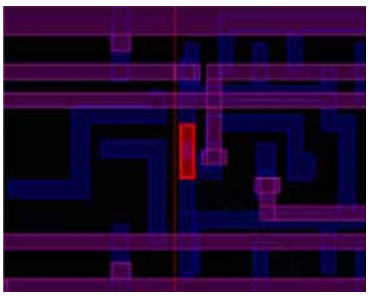
Advanced Node Yield Challenges

As technology advances to 40nm and beyond, designs are being scaled down to meet the ever-increasing demand for more functionality contained in a single chip. Scaling down to smaller geometry poses great challenges on silicon. Lithography, etch, chemical mechanical polishing (CMP), and mask systematic manufacturing variations surpass random variations as the prime limiters to catastrophic and parametric yield loss.

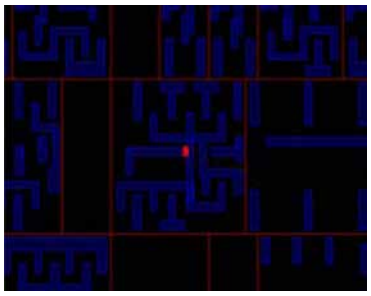
Silicon variability impacts both the physical integrity and the parametric performance of the design. The interaction of manufacturing shapes within the optical proximity halo and the lithography projection systems create highly non-linear systematic variations at different process conditions that cannot be captured by rules-based approaches. The minimum design rule check (DRC) rules fail to capture many potential yield issues, and relaxing DRC rules causes an unacceptable increase in design area. These systematic shape



Spacing bridging



Width pinching



Line end bridging

Figure 1: Different types of yield-detractor lithography hotspots

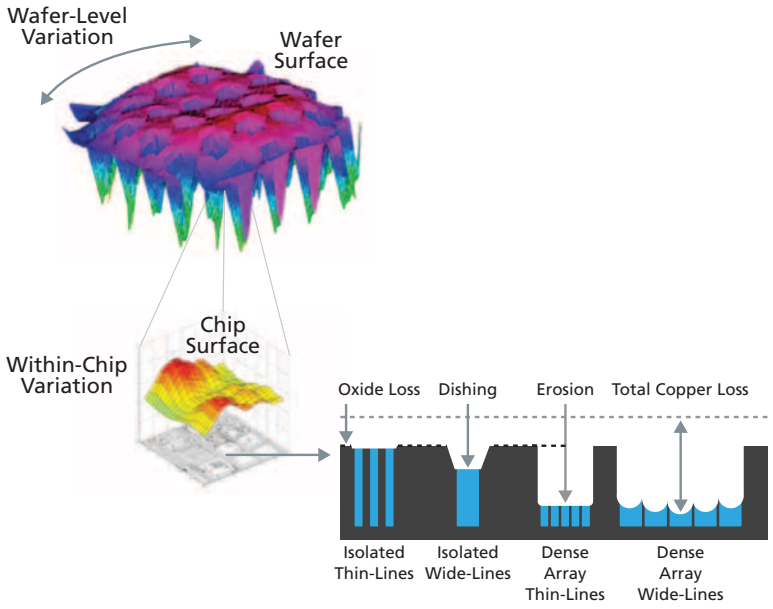


Figure 2: Wafer-level variation due to CMP can lead to topology hotspots or variations

variations are dependent on specific layout shape context, and result in predictable catastrophic errors such as necking (opens) and bridging (shorts). These yield limiting hotspots must be detected and fixed prior to tapeout.

The CMP process introduces issues such as dishing and erosion, which can lead to potential yield and performance problems including copper pooling and excessive copper loss. Rule-based dummy-fill insertion or tiling is done on the design database prior to tapeout. However, in advanced CMP processes, wide wires can experience more dishing than narrow wires, and in some layout configurations narrow wires can be shorted when they are on top of two large plates due to the extra residue from the large plates. CMP can also impact lithography. Areas with high or low surface height can cause defocusing issue in the above layers; hence, severe topography variations can cause printability issues.

Because of increasing design costs and time-to-market pressures, a re-design or a few-weeks' delay caused by poor yield can result in the loss of a critical market window opportunity.

Design For Manufacturing (DFM)

The motivation on the manufacturing side is clear; good DFM enables early ramp to good yield or the fastest time to market for a design.

DFM checks bring manufacturing-awareness to the IC design flow. The most essential one is lithography process check (LPC) to detect and correct systematic litho yield-limiting issues during design. Model-based litho hotspot detection is silicon-accurate and can validate design manufacturability and account for complex two-dimensional lithography and mask effects. LPC also provides design teams with invaluable early insights and allow them to reduce physical variability that could severely impact the performance of the design. With DFM tools integration into digital and custom implementation flows, a unified DFM flow consisting of model-based lithography checks and model-based CMP checks can deliver early prevention, detection, and fixing, so as to meet the stringent design cycle times.

Turnkey litho and CMP hotspot analysis service for 40-28nm designs

Cadence offers best-in-class DFM services that include LPC and CMP verification for 40nm to 28nm nodes. The goal is to enable design teams to effectively detect yield-limiting litho or CMP hotspots and fix them during the IC design phase prior to tapeout.

Litho process check (LPC)

LPC predicts the silicon image of the design shapes and detects where the fidelity between silicon and design intent is problematic, or where print-ability is too challenging and induces too much variability. LPC is model-based and silicon-accurate, and can validate design manufacturability and account for complex two-dimensional lithography

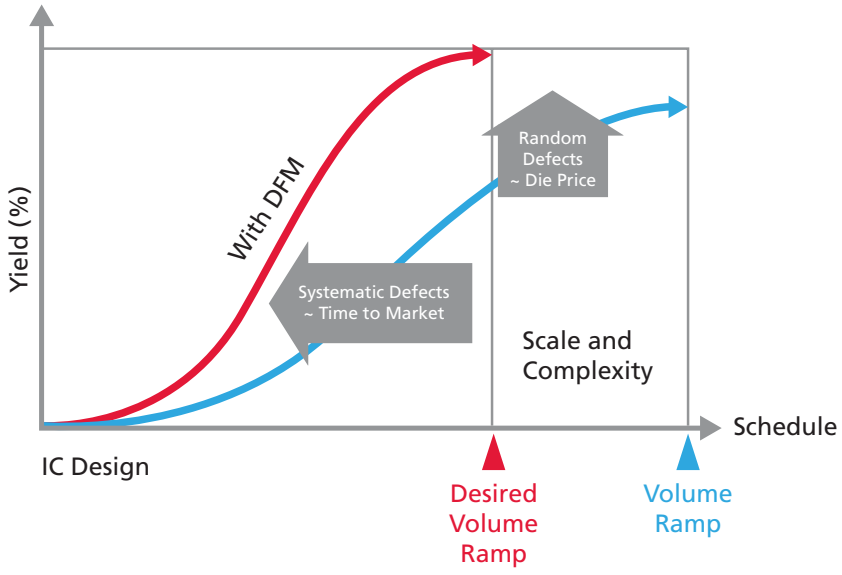


Figure 3: Earlier ramp to yield with DFM

and mask effects. The tool uses a foundry qualified litho model and must simulate all the physical shapes as fast as possible without compromising accuracy. It should identify and reduce design sensitivity by predicting and reducing shape variations. Printability hotspots vary from bridging (short), pinching (open), contact overlap, transistor variations, etc. Design-side litho analysis provides design teams with invaluable early insights and allows them to reduce physical variability that could severely impact yield and the performance of the design.

Chemical mechanical polishing (CMP) check

CMP checks take into account multi-level and long-range effects. CMP hotspots are shown as a density heat map. This helps designers understand the root cause of the CMP issues which are mainly caused by insufficient metal fill implementation or too much variation between high and low density areas of the block or chip. The correction of the density imbalance can be done by incrementally altering the metal fill already implemented manually, or automatically with intelligent fill-aware tools and followed by signoff timing optimization loops.

Flexibility to choose

IC designers can either purchase qualified DFM tools or rely on a qualified DFM service offering. The advantages of owning a tool are obvious, if multiple designs are being developed and machine resources are available.

A **DFM service** model is preferred when a design team desires zero ramp time, minimal tool learning, and no IT burden. This is where Cadence DFM Services aims to deliver the best cost of ownership and technical expertise. Cadence DFM Services team uses foundry-qualified tools: Cadence Litho Physical Analyzer (LPA), the "golden" engine for 40nm lithography process checking (LPC), and Cadence CMP Predictor, the industry-leading CMP analysis solution.

Cadence DFM Services infrastructure uses the latest foundry litho and CMP models for 40-28nm nodes. It leverages the cloud infrastructure and the compute power of hundreds of central processing units (CPUs) assembled to provide timely completion of full-chip LPC or CMP checks on all required layers to deliver the fastest turnaround time. The hardware infrastructure can easily scale to support advanced node design needs—whether it's supporting a few early pipe-cleaner jobs or multiple large designs concurrently. A state-of-the-art IT and security infrastructure further ensure that the customer design data is secure and protected from unauthorized access.

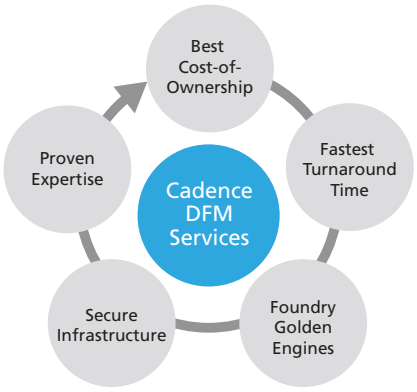


Figure 4: Cadence offers services as well as fully qualified solutions

Leveraging the Breadth of Cadence Expertise

The setup and initiation process is secure and simple. Customers ship their encrypted design database (in GDSII or OASIS format) to a secure, customer-specific drop box, and receive the analysis back within days. The DFM Services team provides consultation and detailed reports, which include the hotspot locations with X, Y coordinates and show deviation from the required width or spacing in a necking or bridge hotspot location. DFM Services also provides layout-modification guidelines for the hotspot, which customers can follow to fix the weak layout topology. The optimal fixing methodology is to leverage the automated fixing flow in custom and digital flows where supported.

The result of the turnkey signoff DFM service provides businesses multiple advantages, including:

- End-to-end DFM signoff analysis, which ensures design manufacturability
- Reduced total cost of ownership for design teams via no investment in DFM tools or multi-CPU IT infrastructure or human time
- Secure infrastructure, which has been tested and is highly reliable and scalable
- Cadence expertise leveraging production-proven tools, methodologies, processes, and use models to provide the fastest turnaround time

Benefits

- Best total cost of ownership: no investment in software tools, multi-CPU infrastructure, or learning new tools
- Efficient access: provides priority turnkey access to foundry "golden" LPC analysis both prior to and at tapeout
- Reduced schedule risk: allows customer to verify block-level LPC and CMP compliance early with a "pipe cleaner"
- Optimal time to results: harnesses 100s of dedicated CPUs/run in our server farm for fast turnaround time
- Security: leverages a highly reliable and state-of-the-art IT and security infrastructure, which ensures protection from unauthorized access
- Leverages Cadence expertise: offers many years of experience and combined resources of Cadence Design Services
- Low-risk learning experience: provides a learning experience for designers to understand DFM while designing with advanced process nodes
- Automated repair: output report enables automated fixing in digital and custom implementation flows

DFM Tool Infrastructure For LPC

Leveraging the foundry "golden" litho hotspot analyzer

DFM Services uses Cadence Litho Physical Analyzer to facilitate the LPC. Litho Physical Analyzer is the silicon-proven, full-chip lithography verification solution that improves manufacturability, yield, and design convergence in the chip design flow. It has been the first to qualify and

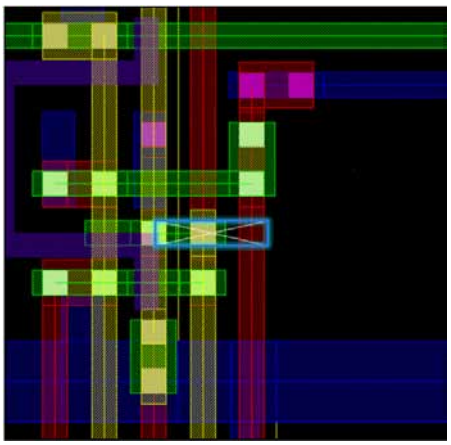


Figure 5: Litho hotspot identified on the design database

Figure 6: Guidelines to help designers fix the identified yield detractor hotspots

meet the accuracy requirements and is the "golden" engine at the world's leading foundry for the 40nm process node.

CMP Check With Cadence CMP Predictor

CMP Predictor provides full-chip, multi-level interconnect topography predictions for the copper CMP process. Cadence CMP Predictor accurately predicts the impact points or hotpsots, like copper pooling for example, and how they can be minimized during the design process.

Areas with high or low surface height can cause defocusing issues in the above layers. For these reasons, severe topography variations can cause print-ability issues. DFM Services' CMP analysis reports help designers understand the root cause of CMP issues, which is mainly due to insufficient metal fill or too much difference between high- and low-density areas of the block or chip. The density imbalance can be corrected by incrementally altering the metal fill manually or automatically with intelligent fill-aware tools and followed by signoff timing optimization loops.

Summary

Cadence DFM Service includes:

- Litho process check (LPC) for 40-28nm nodes
  - LPC is run on cells, blocks, and full-chip SoCs
  - Comprehensive report includes hotspots and locations
  - Design layout fixing guidelines for use with third-party implementation tools
  - Output file for automated fixing with Encounter and Virtuoso tools
  - Incremental re-check to ensure no new hotspots have been created
- Chemical mechanical polishing (CMP) check for 28nm
  - Run on blocks (>1mm2) and full-chip SoCs
  - Comprehensive report with topology hotspots and locations
  - Design layout fixing guidelines
  - Output file for automated fixing with physical verification/DRC tools
  - Incremental re-check to ensure no new variations have been created

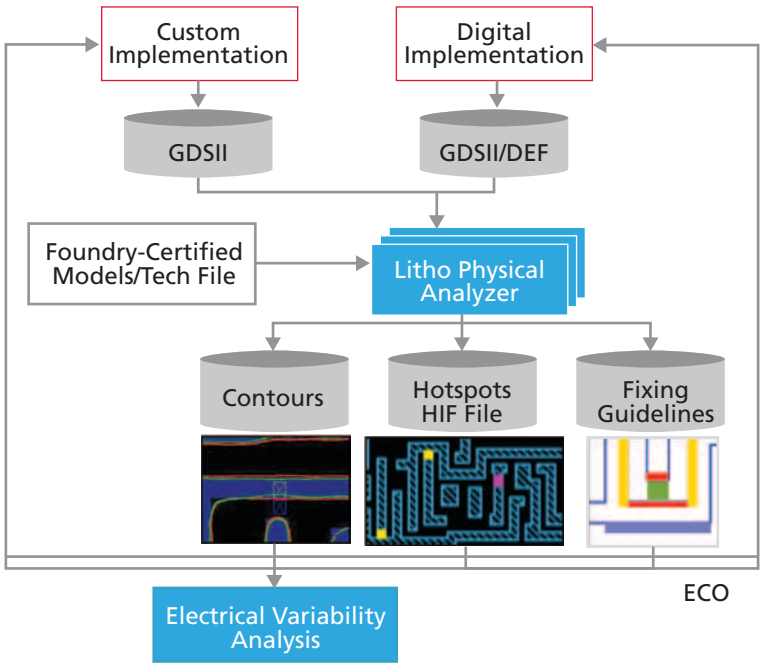


Figure 7: Litho Physical Analyzer supports both digital and custom litho analysis

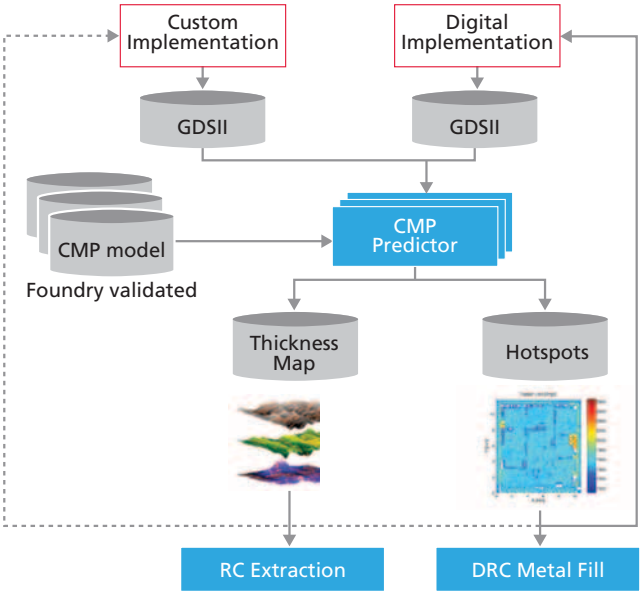


Figure 8: CMP Predictor performs model-based CMP analysis

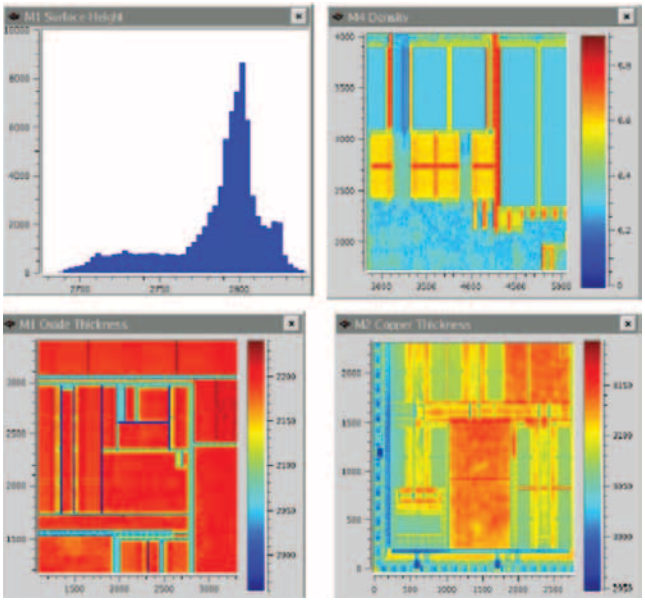


Figure 9: Sample outputs from CMP Predictor

More Information

To get more information on how we can customize our services for you, please email us at dfmservice@cadence.com

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Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. **www.cadence.com**

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