Designing Out DFM Issues at 65nm

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Introduction

- Overview of S3
- What is DFM ?
- Why DFM is an issue now ?
- How can we improve our designs for DFM?
- Conclusions

About S3

- **Consumer Electronics Design Company**
  - Home Entertainment
  - Mobile Multimedia
  - Healthcare

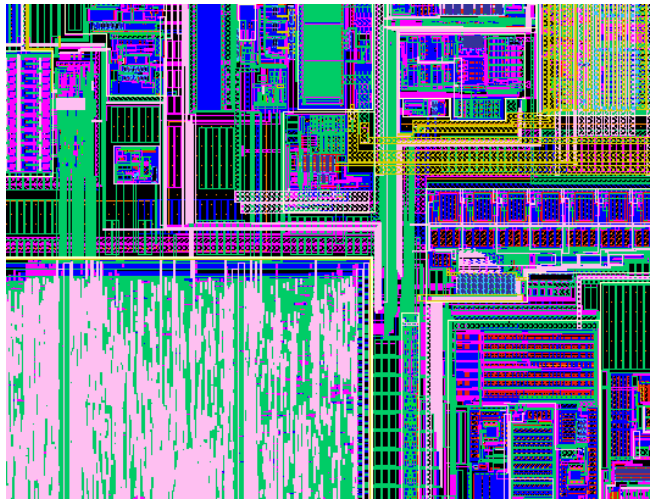
- **Integrated Circuits and Embedded Software Solutions**
  - Worldwide Client Base

- **Getting Clients to Market Faster**
  - Expertise, Innovation, Products, Process

MEDICAL DESIGN EXCELLENCE AWARDS®
SUPPLIER TO A 2005 WINNER

S3 - Nanometer Leadership

- **Global Leader in Nanometer IC Design**
  - On schedule right first time silicon
  - Mixed Analog / Digital SoC Focus
  - Over 25 Designs in 90nm
  - Developing in 65nm since 2004



- **Serving Top Tier Clients**
  - Including Atmel, Philips, Micronas Texas Instruments, Toshiba

- **Teaming with Leading Technology Partners**
  - Including Cadence, IBM, Synopsys, TSMC

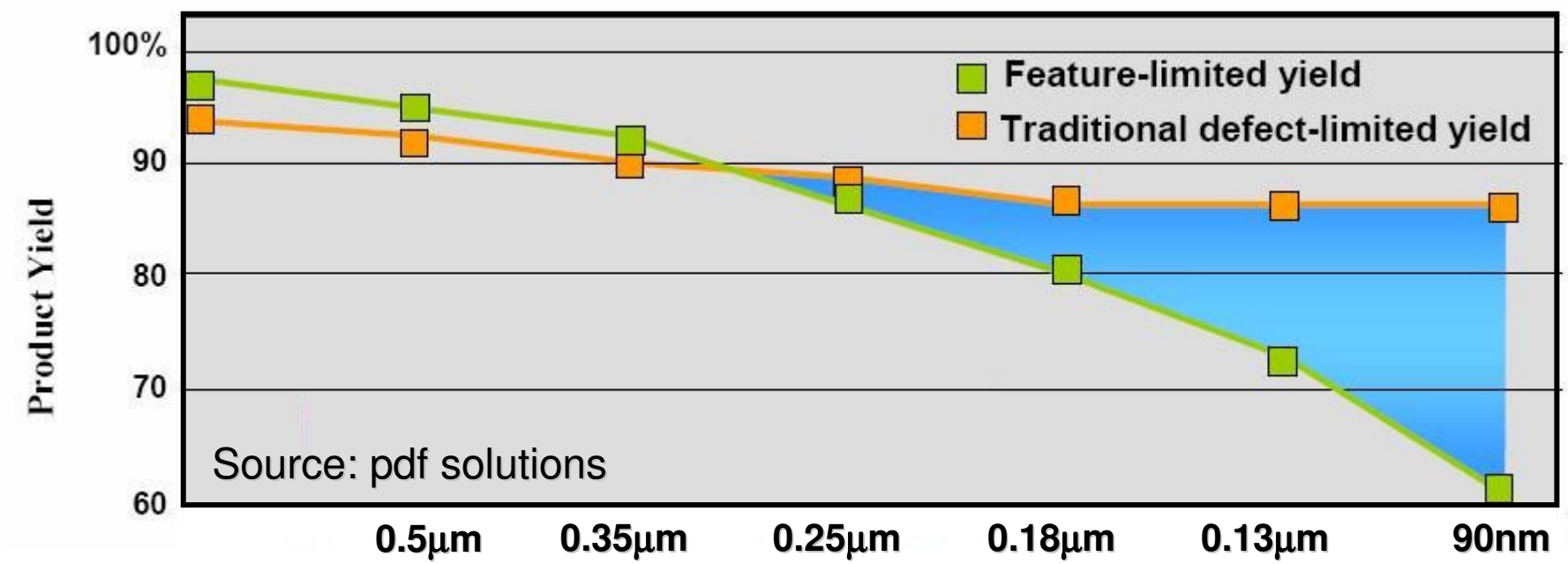
What is DFM?

- Yield quantifies successful silicon die throughput
- DfM / DfY tackles known yield issues by best design practice
- Yield implication for unit $cost:

$$\$unit = \frac{\$wafer}{(\#die) \times yield} + test\_time \times (\$tester)$$

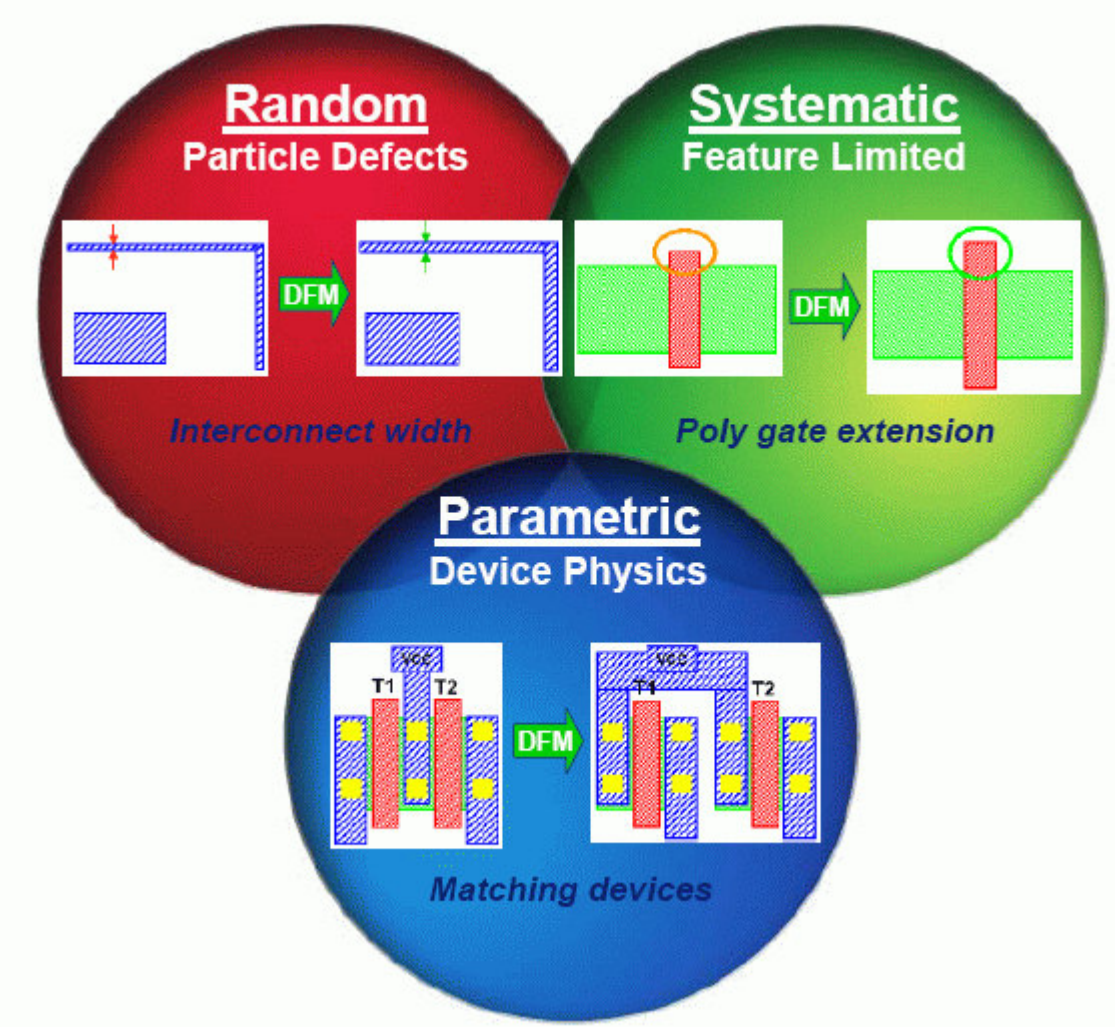
- Ultimately impacts the ROI for the IC vendor

Design for Manufacture

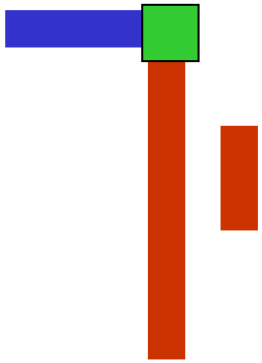


- **Trend getting worse for 65 / 45nm**
- **90nm feature size created by 193nm lithography**
  - "Like painting a thin line with a thick brush"
- **Best design practice captured by working at leading edge technologies**

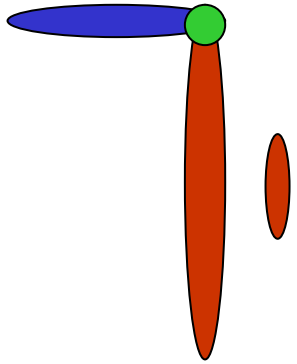
Types of Yield Loss?



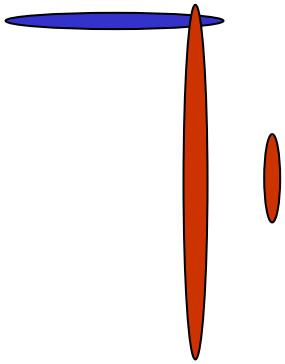
Why is DFM an issue now at 65nm?



Drawn in Layout tool

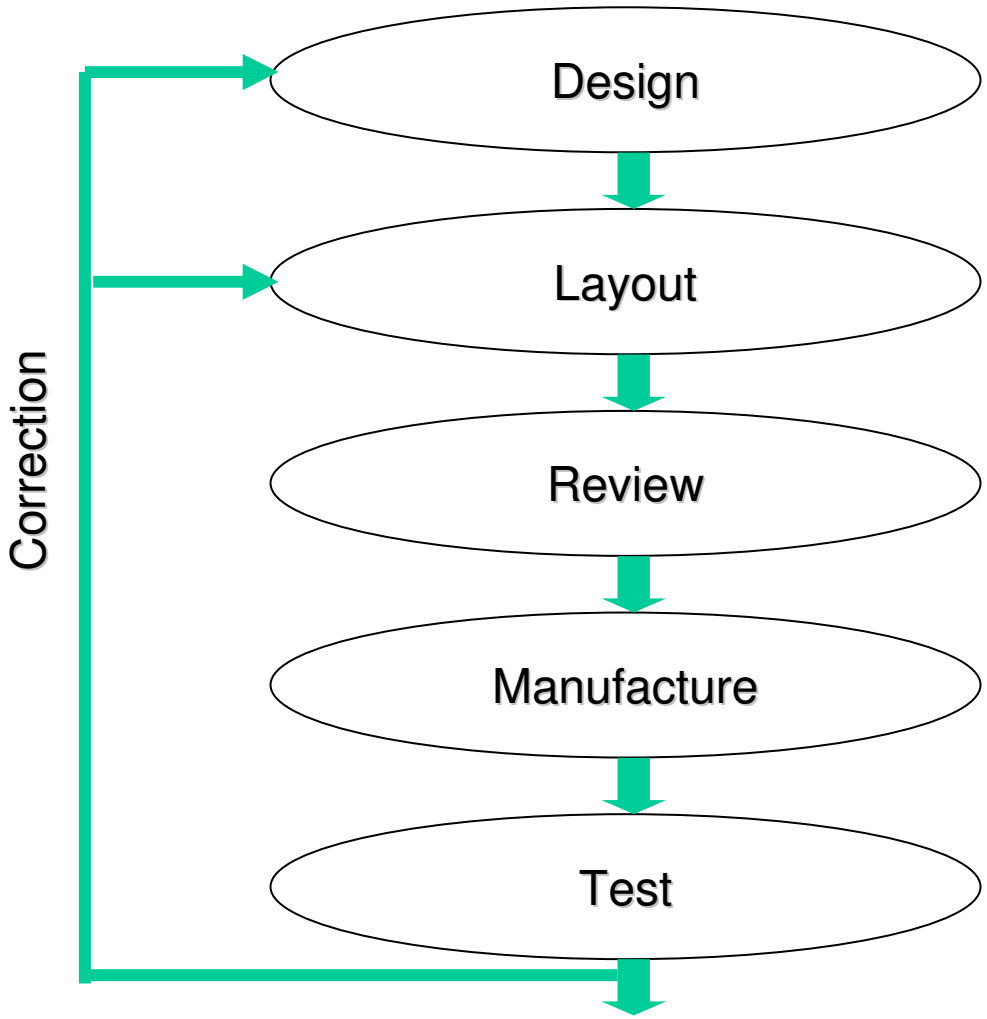


Manufactured
at older technology
nodes



Manufactured
at 65nm

How Can We Improve Our Designs For DFM?



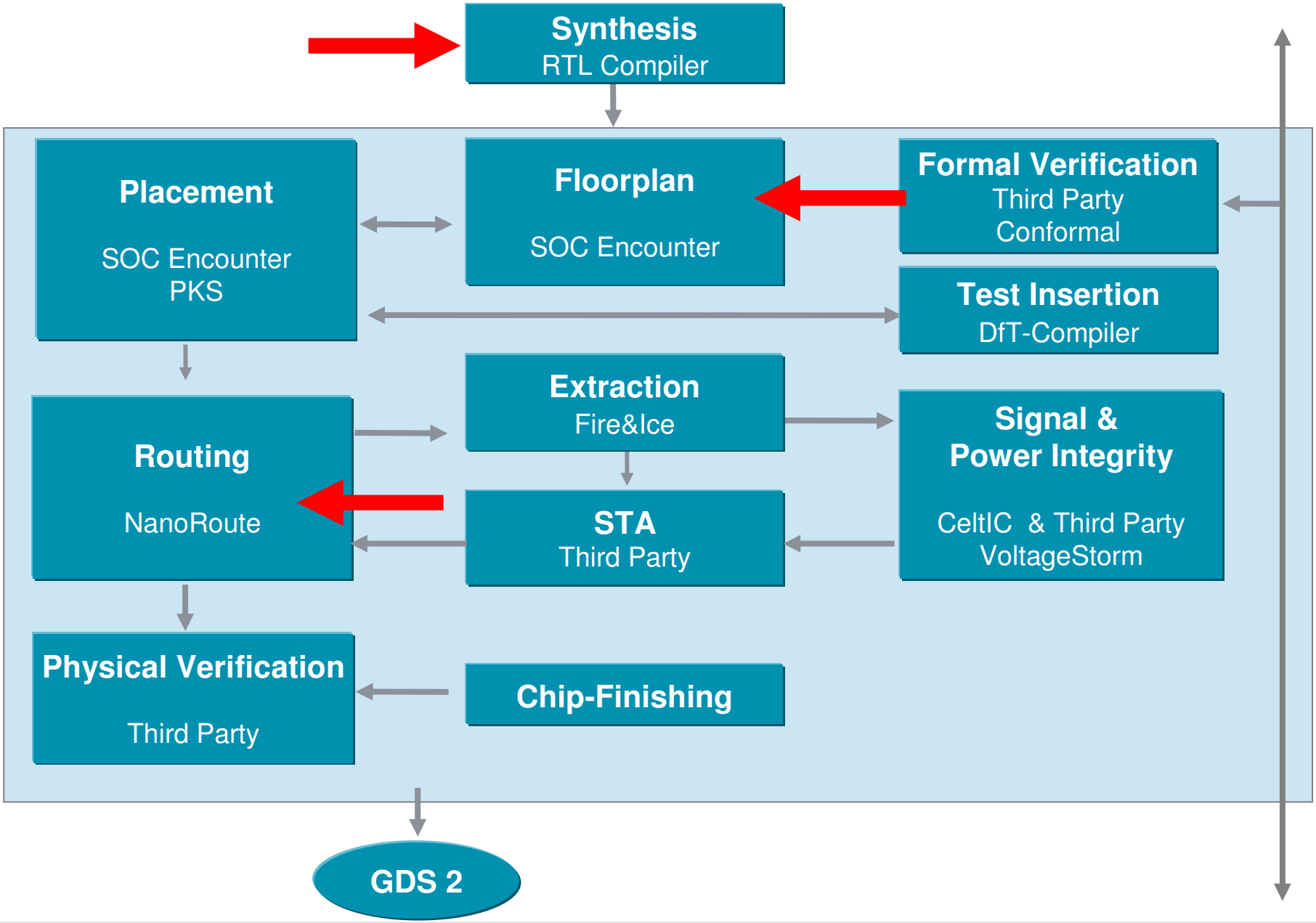
Redundancy, testability, libraries, IP, etc

Robust layout: Library / re-usable IP, foundry yield analysis

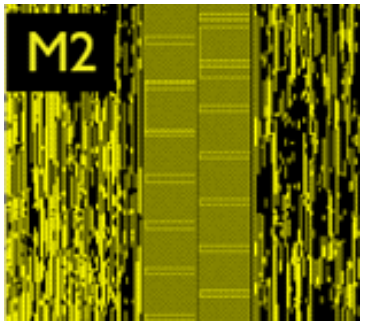
Maturity consideration

Failure mechanism analysis

DFM Aware Design Flow

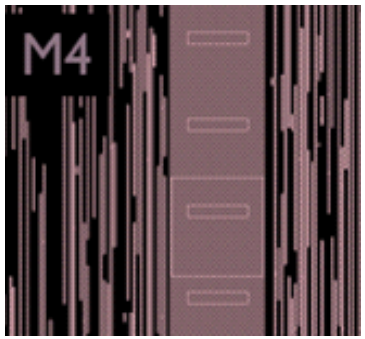


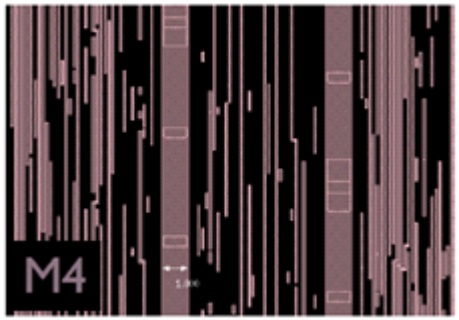
DFM Aware Power Grid



Non DFM aware

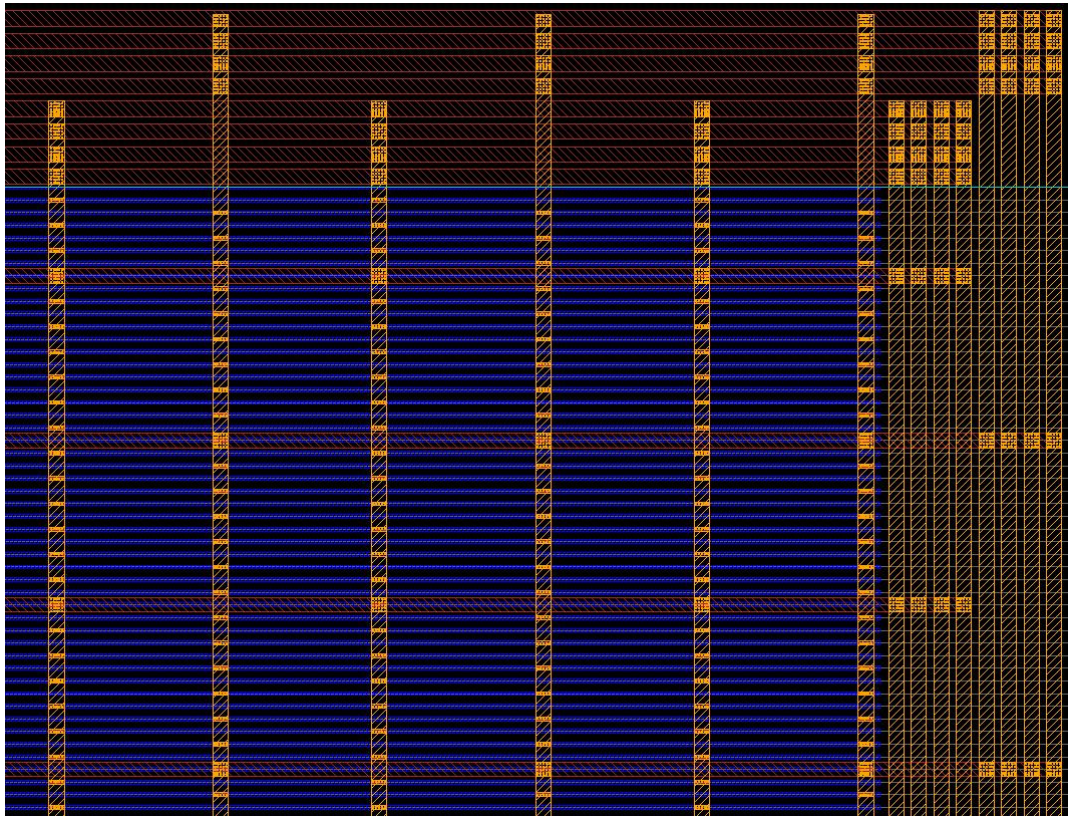
DFM aware



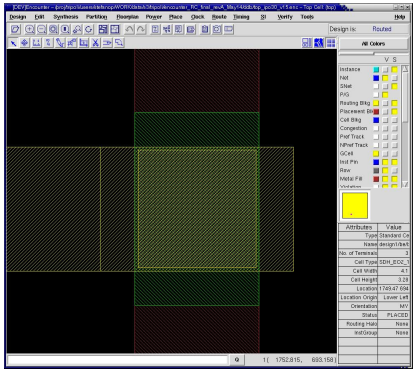


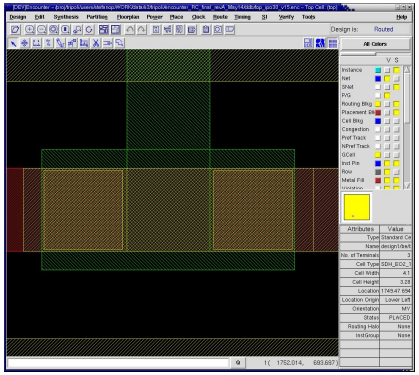
S3 Approach

- Even VDD / VSS grid
- Conditional spacing
- Wide track minimisation



Via Doubling



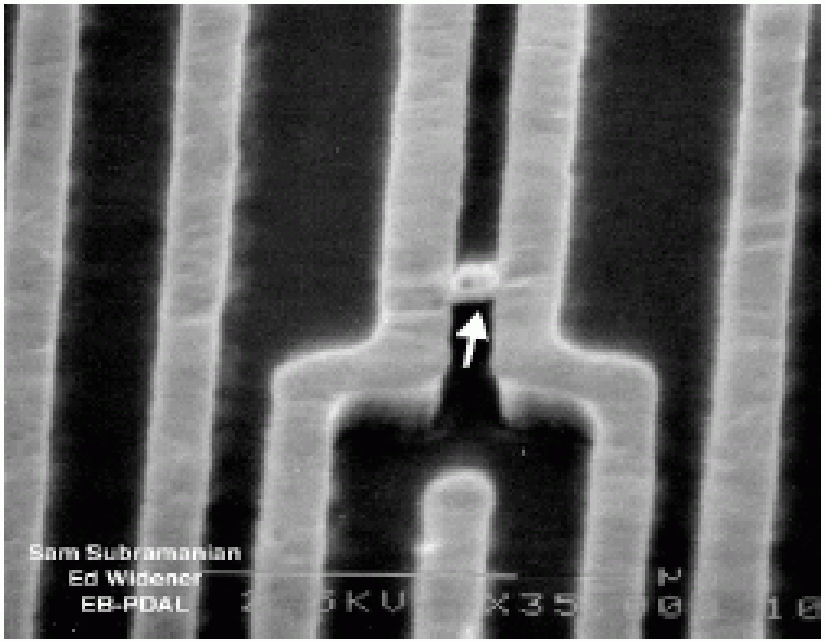


- **Risk**
  - High resistivity on single vias
- **Identify single vias on critical nets**
  - e.g. With respect to timing or matching
- **Doubling vias reduces faults**
  - 50% probability reduction
- **Post-route doubling**
  - Don’t compromise area

S3 Approach

```
 1 Pre multi-cut via insertion:
 2
 3 #                    single-cut          multi-cut      Total
 4 #--------------------------------------------------------------
 5 #  Metal 1      734920 ( 99.9%)       432 (  0.1%)     735352
 6 #  Metal 2      778059 ( 99.9%)       551 (  0.1%)     778610
 7 #  Metal 3      440994 ( 99.9%)       370 (  0.1%)     441364
 8 #  Metal 4      240562 ( 99.9%)       227 (  0.1%)     240789
 9 #  Metal 5       88830 (100.0%)        11 (  0.0%)      88841
10 #--------------------------------------------------------------
11 #              2283365 ( 99.9%)      1591 (  0.1%)    2284956
12 #
13
14 Post multi-cut via insertion:
15
16 #                    single-cut          multi-cut      Total
17 #--------------------------------------------------------------
18 #  Metal 1      274948 ( 37.4%)    460404 ( 62.6%)     735352
19 #  Metal 2      176205 ( 22.6%)    602405 ( 77.4%)     778610
20 #  Metal 3       96677 ( 21.9%)    344687 ( 78.1%)     441364
21 #  Metal 4       43947 ( 18.3%)    196844 ( 81.7%)     240791
22 #  Metal 5       17151 ( 19.3%)     71690 ( 80.7%)      88841
23 #--------------------------------------------------------------
24 #               608928 ( 26.6%)   1676030 ( 73.4%)    2284958
25 #
26
```

Wire Spreading



Metal particle causing a short

S3 Approach

- **Wire Spreading:**
  - Avoids congestion
  - Benefits both DFM and SI

- **S3 Strategy**
  - Use SOCEncounter SI awareness switches
  - Route clock nets, top level nets and sensitive signals on double spacing

Conclusions

- **Early in the Design Phase**
- **Foundry/Designer Collaboration**
- **Better Solutions for DFM from EDA Vendors**
- **DFM is a Business Opportunity**
  - 5% increase in yield is worth $50M over the life of a cell phone

- **Visit S3 at Stand #05 or www.s3group.com for more information on our leading edge SoC Design capabilities and silicon proven 90nm Mixed Signal IP**