cadence®

Encounter RTL Compiler Advanced Physical Option

Physically aware synthesis for faster convergence on goals

Cadence® Encounter® RTL Compiler Advanced Physical Option delivers real physical interconnect timing to the logic synthesis environment. Its high-capacity global synthesis, combined with the production placement technology enabled by Encounter Digital Implementation System, helps logic design teams easily predict, visualize, and fix physical issues that affect closure on a project's performance, power, and area intent. Encounter RTL Compiler Advanced Physical Option speeds physical design closure by improving predictability and convergence on silicon quality goals through a robust suite of physically aware (PA*) features.

Encounter RTL Compiler Advanced Physical Option

For timing-critical logic, the delay contribution from interconnect is now much larger than that from the gates themselves. Logic designers have been forced to build-in significant timing margins to account for this uncertainty. This extra margin comes at a cost in terms of power and area that cannot be fully recovered during physical design when real wires are available. And at 65nm and below, this cost has become too high.

Encounter RTL Compiler Advanced Physical Option seamlessly adds real physical interconnect timing to the global synthesis process by placing the cells within the production floorplan. This approach allows logic designers to maintain the same logic synthesis use model, environment, and abstraction level, but with physical reality built-in. The result is increased accuracy in the factors that synthesis optimizes, enabling the best balance of performance, power, and area—and with the appropriate amount of physical feedback as it pertains to logic design and synthesis. By raising the physical design context to the earliest stages of the synthesis flow (structuring, mapping, etc.), Encounter RTL Compiler Advanced Physical Option can provide the earliest possible insights into physical effects that will impact the design during place and route, and address many of those challenges in a runtime- and productivity-efficient stage of the digital flow.

Benefits

Improves predictability of physical design closure

- Realistic interconnect timing in synthesis means that when goals are met in synthesis, they will also converge in physical design
- Handoff of legal placement enables the physical design team to start with exactly the same model on which the logic design team signed off
- Modeling routing congestion during synthesis at a higher level of abstraction helps structure logic to avoid actual congestion issues later in the routing stage

Increases overall quality of silicon

- Accurately focuses performance optimization on the truly timing-critical logic through RTL-level Physically Aware Mapping (PAM)
- Predicts and eases congestion in datapath-intensive designs by using Physically Aware Structuring (PAS)

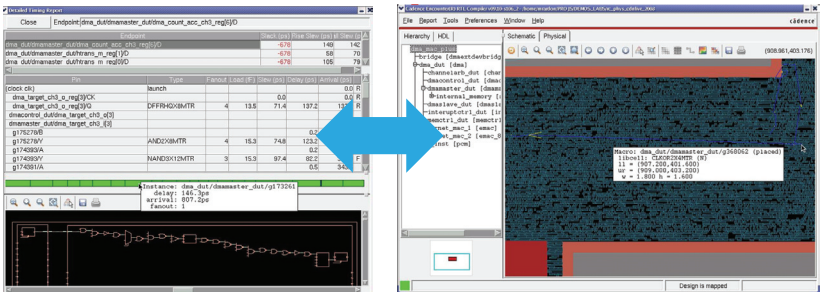

Figure 1: View timing paths with physical interconnect knowledge built-in, and cross-probe to the physical viewer to see associated wire lengths

- Reduces power consumption by eliminating the need to apply excessive performance margin
- Lowers clock power without impacting timing/congestion by merging single registers into multi-bit registers through Physically Aware Multi-Bit Cell Inferencing (PA-MBCI)
- Synthesizing at the physical partition level with abstracted physical interconnect timing enables the broadest scope of optimization
- Performing physical optimizations earlier in the implementation process enables larger-scale improvements
- Analyzes and fixes scan chain ordering inefficiencies and reduces ATPG compression/decompression congestion through Physically Aware Design for Test (PA-DFT)

Reduces schedule risk

- Eliminates iterations between logic and physical design teams caused by large differences in interconnect timing models
- Provides early insight into potential congestion issues that can occur during routing

Ease of use enables widespread adoption by logic designers

- Utilizes the same synthesis use model and user interface to which logic designers are accustomed
- Physical interconnect modeling gives logic designers early insight into problems physical designers will encounter, enforcing smarter RTL design
- Increases communication between logic and physical design teams

Features

Encounter RTL Compiler Advanced Physical Option

Encounter RTL Compiler Advanced Physical Option brings the production placement engine of Encounter Digital Implementation System into the Encounter RTL Compiler global synthesis environment, enabling a physically aware reference point for each stage of synthesis.

- Encounter Digital Implementation System placement runs automatically as part of synthesis
- Physically Aware Structuring (PAS)
- Physically Aware Mapping (PAM)
- Physically Aware Multi-bit Cell Inferencing (PA-MBCI)
- Physically Aware Design for Test (PA-DFT)
- Physical timing-path viewing helps quickly identify the root cause of timing issues at a higher level of abstraction
- A placement viewer facilitates communication between logic and physical design teams
- Native congestion modeling drives every step of synthesis optimization
- Easy to view, fix, and prevent congestion issues
- Enables physical optimizations, including gate decomposition and composition, buffering, and location assignment
- Delivers physically aware incremental retiming
- Top-down register retiming balances logic across registers, maximizing data throughput in a single-pass synthesis run while writing out compare-point information to enable equivalence checking
- Provides legal placement within power domains defined by the Common Power Format (CPF)
- Superthreading, built-in along with two threads, speeds up overall turnaround time
- Reads LEF library and macro models, and DEF floorplan, including pre-placed cells, blockages, regions, fences, etc.
- Writes out legal placement (DEF) to seed physical implementation and accelerate design convergence

Encounter RTL Compiler global synthesis

Built from the ground-up from algorithms that address today's design challenges, Encounter RTL Compiler delivers the best quality of silicon in terms of performance, power, and area measured with wires. Its unique algorithms enable chip-level capacity and fast runtimes, greatly improving synthesis productivity and results. True multi-objective optimization simultaneously optimizes performance, power, and area intent, speeding convergence on the optimal balance of your design goals.

For more information, please consult the Encounter RTL Compiler datasheet.

Specifications

- Linux (32-bit, 64-bit)
- Sun Solaris (64-bit)
- IBM AIX (64-bit)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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