Cadence InCyte Chip Estimator

Fast and accurate estimation of IC size, power, performance, and cost

Cadence® InCyte™ Chip Estimator is a unique coupling of software and an IP ecosystem that enables rapid and accurate early chip planning. Fast "what-if" estimation of size, performance, power, and cost enables early exploration of functional content, IP components, memories, and process technology with foresight into the technical and business consequences of these decisions. InCyte Chip Estimator helps chip design projects start and stay on track toward their technical and business goals.

With the escalating costs of chip design, it is imperative that projects begin with careful planning to ensure that goals can be met and monitored for progress. Cadence InCyte Chip Estimator combines breakthrough size, performance, and power estimation algorithms with the industry's largest collection of IP to enable accurate what-if analysis that explores both technical and business feasibility.

Closing early on a system-on-chip (SoC) specification that meets project goals and gaining insight into downstream technical implementation reduces overall project risk and speeds the project's time to market. InCyte Chip Estimator's fast, accurate, and simple-to-use environment helps any user achieve optimal results without being an IC design expert. It can be used by technology team members (design architects, chip integrators, design leads, engineering management) as well as business team members (field sales consultants, technical marketing, IC component procurement, RFQ response, executive management) to plan, estimate, and track chip design projects. This is useful for fabless semiconductor companies, integrated device manufacturers, ASIC vendors and customers, design services providers, and IP providers.

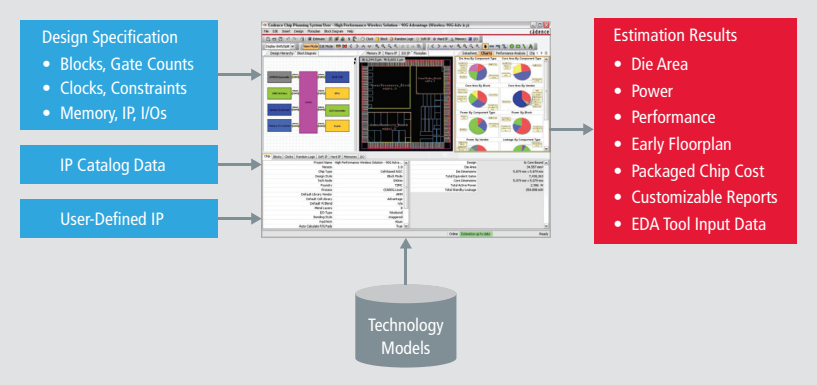

Figure 1: Size, performance, and power estimation algorithms combined with an extensive IP catalog enable early and accurate what-if analysis

Benefits

- Improves predictability of success
  - Closes early on a specification that best balances size, power, and costs
  - Uses real IP, process, and architecture data to determine specifications
- Addresses the impact of power comprehensively
  - Estimates power at the architectural level
  - Plans block-level and chip-level power strategies
  - Models different power modes
  - Generates a Common Power Format (CPF) file to drive downstream implementation
- Provides access to ChipEstimate.com, the foremost IP ecosystem
  - 7,000+ IP components from 200+ IP suppliers and foundries
  - Compares digital, analog, and mixed-signal IP in the context of your design, before contacting multiple IP providers directly

  - Provides a wide set of design options to explore
- Quantifies the cost impact of chip architecture and implementation decisions
  - Draws on built-in economic and yield data
- Reduces implementation risk
  - Enables early planning followed by a convergent flow
  - Passes architecture and library data forward to drive implementation tools
  - Feeds back implemented block data to refine accuracy of the model and to drive in-project decisions
- Ease-of-use enables collaboration
  - Promotes communication among business and technical teams
  - Starts with early planning and continues throughout the course of the project

Features

Cadence InCyte Chip Estimator operates in a client-server model and has the libraries you need already built-in. The client is the InCyte Chip Estimator application on your Windows or Linux desktop. The server brings that same IP catalog and foundry libraries from ChipEstimate.com directly into the client application. InCyte Chip Estimator is available in several different configurations.

InCyte Chip Estimator L

For accurate technical estimation of design size and power, InCyte Chip Estimator L combines foundry-specific models with the ChipEstimate.com IP portal inside an easy-to-use estimation environment.

- Access the ChipEstimate.com IP catalog (built into the software)
- Select foundry-specific foundation libraries of standard cells, I/Os, and memories.
- Select a specific foundry library at a specific process node
- Filter the built-in IP catalog to show IP suitable for that node
- Define custom IP macros
- Estimate design size
- Estimate design power (dynamic and leakage)
- Compare size, power, and performance of multiple designs or design variations
- Estimate performance achievability in specific manufacturing processes with specific IP components
- Create and edit a block diagram of the design using drag-and-drop for blocks and drawing tools for connectivity
- Edit the floorplan view to analyze impact of movement and rotation on size, power, performance, and cost
- Export the design intent downstream to synthesis, low-power verification, and physical implementation: DEF, LEF, high-level Verilog®, CPF, SDC, synthesis scripts, implementation scripts, and compiled memory scripts

InCyte Chip Estimator XL

InCyte Chip Estimator XL adds advanced analysis capabilities, including economic analysis, power profile analysis, and power management, on top of the core chip planning features of the L edition.

- View economic lifecycle tables and graphs that offer cost analysis of yield-affected wafers, packaging, test and assembly, and non-recurring engineering (NRE) charges
- Generate complete IC economic analysis reports and budgetary quotes
- Create power profiles with various modes, assign percent active time for modes
- Easily include advanced power management techniques (power shutoff, multi-supply/multi-voltage, clock gating) while measuring the size and power impact of these techniques
- Automatically takes into account the cost overhead of advanced low-power techniques
- Visualize the impact of techniques on dynamic power, leakage power, size, and performance
- Interfaces bi-directionally with Cadence Encounter® RTL Compiler synthesis solution
  - Feeds forward SDC, module definitions, floorplan hints, and synthesis scripts
  - Feeds back synthesized gate counts of random logic blocks and compares to earlier estimates
- Interfaces bi-directionally with the Encounter Digital Implementation System
  - Feeds forward SDC, floorplan hints, and implementation scripts
  - Feeds back implementation metrics to enable economic analysis and compares to earlier estimates
- Interfaces with Spirit IP-XACT for import/export
- Supports control and extensibility of chip planning with Python shell interpreter

InCyte Starter Edition

A free version of InCyte technology, the Starter Edition, is available for download to demonstrate how ChipEstimate.com and InCyte work together. The data in this version is limited to industry averages instead of specific processes, so it should not be used for production design. The industry-average data is supported down to the 65nm process node.

- Access the Chip Estimate.com IP catalog built into the tool
- Select foundation libraries of standard cells, I/Os, and memories set to industry averages for process nodes
- Define custom IP macros (limited number)
- Estimate design size
- Estimate design power (dynamic and leakage)

InCyte Enterprise Edition

For companies with large amounts of in-house IP to share across geographically diverse development centers, Cadence offers an enterprise solution in the form of the Cadence Chip Planning System. It includes an in-house corporate server

along with the Chip Planning System client that has all the functionality of InCyte Chip Estimator XL. It includes an IP modeler that populates the enterprise's own IP, and optionally the standard ChipEstimate.com IP, into their own version of the server.

For more information on this edition, please consult the Cadence Chip Planning System datasheet.

System Specification

- Windows XP, Windows XPpro, Windows Vista
- Linux (32-bit, 64-bit), RHEL 4.0, 5.0, SLES 10, 9
- Sun Solaris (32-bit, 64-bit), Solaris 10

Visit www.ChipEstimate.com to register and search through 7,000 pieces of IP from more than 200 IP providers and foundries.