Encounter RTL Compiler

Concurrent optimization of timing, area, and power intent

A key technology of the Cadence® Encounter® digital IC design platform, Encounter RTL Compiler offers a unique set of patented global-focus algorithms that perform true top-down global RTL design synthesis to accelerate silicon realization. With concurrent multi-objective optimization (timing, area, and power intent) and support for advanced low-power design techniques, Encounter RTL Compiler reduces chip power consumption while meeting frequency goals.

Encounter RTL Compiler

With its combination of breakthrough algorithms, efficient data structures, and modern programming techniques, Encounter RTL Compiler delivers the best speed, area, and power after physical implementation for the most challenging designs. New advanced global synthesis technology further improves these results while delivering even faster runtimes. At the core of Encounter RTL Compiler is a breakthrough synthesis algorithm—global-focus mapping (GFM). This technique devotes more time to examining the overall solution space to deliver an optimized netlist for meeting your design intent goals throughout physical design.

Encounter RTL Compiler performs multi-objective optimization that simultaneously considers timing, power, and area intent to create logic structures that converge on all these goals in a single pass. New Encounter RTL Compiler synthesis techniques address today's advanced chip design needs, such as:

- Improved timing, or where a difficult layout demands a solution to meeting/closing timing
- Decreased power (both dynamic and leakage) without sacrificing performance
- Reduced die size
- Better productivity and design turnaround time

Encounter RTL Compiler technology is available though base L or XL, and optional Low Power, Advanced Physical, and CPU Accelerator offerings.

Benefits

- A well-balanced logic structure isolates critical paths, reduces power, area, and congestion in off-critical logic, and enables faster timing closure and design convergence through place and route
- Spatial technology eliminates the need for wireload models by modeling physical interconnect at a higher level of abstraction for use in RTL-to-gate optimization
- Encounter RTL Compiler with Advanced Physical Option incorporates Encounter Digital Implementation System silicon virtual prototyping technology into synthesis, providing real physical timing to logic optimization and analysis
- Reduces power consumption through single-pass multi-Vt optimization, hierarchical and multi-stage clock gating, true top-down multi-supply voltage exploration and synthesis, and full power shutoff support with the Common Power Format (CPF)
- Shrinks die sizes with multi-objective optimization, which creates smaller logic structures for non-timing-critical regions
- Multi-mode synthesis optimization and analysis accelerates overall turnaround time to design closure for complex chips with multiple functional modes
- Superthreading technology leads to superior runtimes, quicker turnaround times, and faster convergence on design goals

- Superior capacity increases productivity by enabling chip-level synthesis and eliminating manual partitioning, budgeting, and reassembly
- A built-in design quality analyzer identifies pre-synthesis design issues that may lead to sub-optimal or unintended results
- Easy to adopt using standard inputs and outputs so that customers requiring improved quality of silicon (timing, area, and power after wires) can quickly achieve their design goals

Features

Encounter RTL Compiler XL

The flagship Cadence synthesis product, Encounter RTL Compiler XL includes all of the features needed to make an existing synthesis environment capable of delivering smaller, faster, and lower-power chips in less time.

- Supports 4M-gate top-down compilation on 32-bit machines; unlimited capacity on 64-bit machines
- Spatial technology models physical interconnect information during global RTL synthesis
- Enables single-pass multi-Vt leakage power optimization
- Enables dynamic power reduction via multi-objective optimization, hierarchical and multi-stage clock gating, and operand isolation
- Performs gate-level power analysis for both average and peak power
- Includes built-in high-performance datapath and arithmetic optimization
- Supports a full suite of ChipWare building-block IP components
- Leverages ChipWare Developer IP infrastructure
- Offers a full, built-in timing engine
- Performs total negative slack (TNS) optimization
- Performs test insertion and scan stitching
- Performs testability rule analysis and fixing
- Design quality analyzer checks for potential issues with RTL, libraries, timing constraints, power specifications, DFT rules, and clock domain crossing
- Read/write standard I/Os include Verilog, VHDL, SystemVerilog, CPF, SDC, and Liberty
- Offers a standard, simple, intuitive, and user-extensible Tcl interface
- Super-threading delivers a runtime speedup proportionate to the number of processors used while delivering the same quality of silicon as a single processor job

Products

Encounter RTL Compiler L

Encounter RTL Compiler L offers the ultimate in flexibility for design teams. It contains all the features and optimization capabilities of Encounter RTL Compiler XL in a configuration designed for runs of up to 100K mapped instances, making it ideal for block-level designers.

You can also accumulate Encounter RTL Compiler L licenses for larger capacity runs—each additional L license increases instance capacity by 100K, and four L licenses combined offer unlimited capacity. This means that block-level designers can use individual Encounter RTL Compiler L licenses, then combine them for chip-level builds while benefiting from the same high quality of silicon delivered by Encounter RTL Compiler XL at every step.

Encounter RTL Compiler Advanced Physical Option

For chips with complex floorplans where physical effects hinder design closure, Encounter RTL Compiler Advanced Physical Option utilizes Encounter Digital Implementation System placement technology to deliver physical timing information to the synthesis environment.

- Performs global synthesis optimization using real physical wire delay during structuring and mapping
- Eliminates the need to add excessive timing margin during synthesis, enabling further power and area reduction
- Presents physical feedback to logic designers to help drive corrective action during synthesis
- Native congestion modeling enables automatic congestion optimization, analysis, and fixing
- Top-down register retiming balances logic across registers, maximizing data throughput in a single-pass synthesis run while writing out compare-point information to enable equivalence checking

Encounter RTL Compiler Low-Power Option

Encounter RTL Compiler Low Power is an option that works in conjunction with Encounter RTL Compiler L and XL, adding breakthrough technologies that address emerging chip design demands. The Low Power option gives designers the power of advanced methodologies with minimal methodology overhead.

- Supports the CPF to specify advanced power intent and reduction techniques across design, verification, and implementation domains
- Performs RTL power estimation and profiling for both average and peak power
- Enables true top-down multi-supply/multi-voltage (MSMV) synthesis, so that designers can match voltage levels with required performance, synthesize the whole chip top-down with multiple voltages, and hand-off domain and level-shifter information to physical design
- Synthesis for power shutoff with isolation and state retention utilizing CPF enables correct-by-construction power logic and optimization

- Multi-mode synthesis simultaneously analyzes and optimizes multiple functional modes, eliminating non-convergent iterations and error-prone manual constraint merging
- Yield optimization adds cell yield as a cost factor during multi-objective optimization, increasing final yield over physical optimization alone

Encounter RTL Compiler CPU Accelerator Option

Encounter RTL Compiler's super-threading capability allows you to reduce synthesis turnaround time by using distributed processing across multiple CPUs. Each Encounter RTL Compiler CPU Accelerator enables two additional server processes that run on available CPUs on the same machine or within the network. Works in conjunction with Encounter RTL Compiler L and XL, which enable one or two server processes respectively.

Platforms

- Linux (32-bit, 64-bit)
- Sun Solaris (64-bit)
- IBM AIX (64-bit)

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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