TECHNICAL PAPER

ENCOUNTER CONFORMAL ECO DESIGNER

Revolutionizing the Art of ECOs

cadence™

OVERVIEW

"Engineering change order" (ECO) is a common term in the semiconductor industry. It has a wide variety of connotations—from adding or removing logic to more subtle changes such as cleaning up routing for signal integrity. An ECO can come at any point in the design cycle, with the goal being to deliver the product to market as quickly as possible with minimal risk to correctness and schedule. Whenever it occurs—and whether it represents a simple design fix or spinning a derivative product—an ECO is widely recognized by engineering and management as a time of high stress, long work hours, and uncertainty.

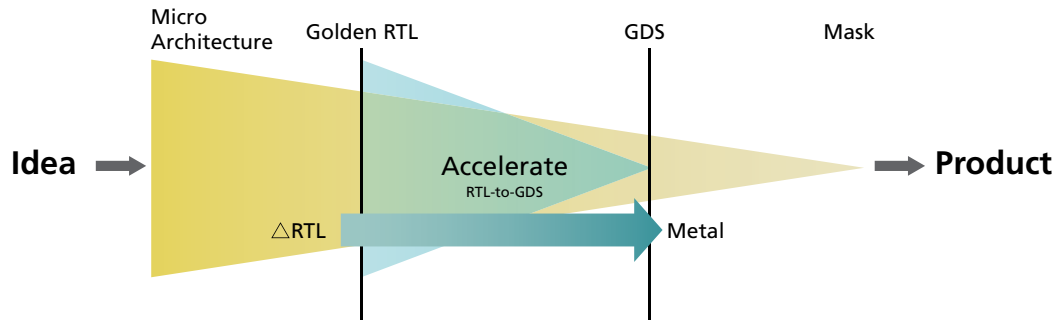

Figure 1: ECO challenge

Today's ECO flows are manual and labor-intensive, and remove only some of the uncertainty regarding whether the product will function properly. Since designers typically don't know if a change made in the logical netlist can be executed in the physical netlist, completing the ECO process typically requires many cycles. However, if designers are provided with early knowledge of the feasibility of implementation, an ECO can be achieved with only metal layer changes, enabling the design team to dramatically reduce cost by changing plans and targeting workable solutions.

The manual process imposes another significant restriction. Keeping track of used spare cells and freed cells with accuracy becomes increasingly difficult when performing changes on several different levels, which makes some ECOs too complex to handle manually.

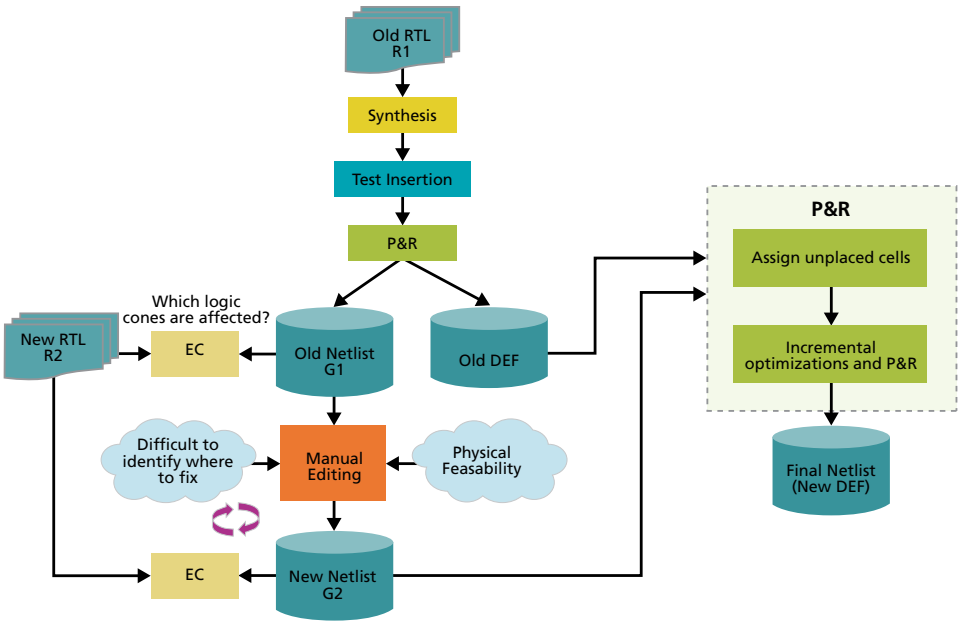

Figure 2: Manual ECO flow

The flow outlined in *Figure 2* represents a typical manual flow. It starts by comparing the old netlist to the modified RTL using an equivalency checker. By looking at the differences, the designer can locate the changes necessary in the netlist. After manual editing and rechecking, the netlist is ready for physical implementation. Typically, there are many time-consuming cycles in this loop (which can be tedious when coupled with the task of keeping track of freed gates and used spare cells). Next, the place and route tool assesses the differences of the modified logical netlist and the physical def file to correct the physical implementation. Finally, the new netlist needs to be compared to the modified RTL. This is not always possible using some equivalency checking tools, which rely on information passed from the synthesis tool.

With mask costs running into the millions of dollars, an ECO can mean the life or death of a project—or even a company. Knowing that an ECO can be implemented with the gates on the mask and then processed with a limited number of metal layers enables a design team to move with confidence and efficiency. By adding more flexibility, chips can be processed through the base levels and several metal layers, and then finished with new ECO metal layers, thereby saving cost and ensuring that time-to-market goals are met.

APPLICATION

PRE-MASK AND POST-MASK

When the ECO is applied, it is important to consider if the state of the design is pre-mask or post-mask. Pre-mask ECOs are performed during place and route and before the design is taped out. Pre-mask ECOs can be broken down into two categories: functional and non-functional. Functional ECOs deal with making logical changes to the design, while non-functional ECOs handle changes that affect timing and signal integrity, such as design rule verification (DRV) or routing. At this point, there is no mask to limit resources utilized, nor is it necessary to keep track of freed cells or utilized spare gates. Post-mask ECOs are performed after the design has been sent to manufacturing. Once fabrication has begun, the number of gates on the die is fixed and any changes will need to be accomplished with these resources. Ideally, a post-mask ECO will be achievable with simple metal layer changes, thereby greatly reducing the cost of the ECO.

ECO FEASIBILITY

Feasibility is another consideration for ECOs. Many customers want to process multiple ECOs but are uncertain if all of the ECOs can be implemented. To increase the level of certainty, designers will perform the ECOs one at a time. However, this strategy causes many projects to run out of schedule, and forces design teams to defer some changes to the next revision of the chip to meet time-to-market considerations. If engineers can determine which ECOs can be implemented, they can focus on the feasible ECOs and proceed to tapeout of the design.

To determine the feasibility, Cadence® Conformal® ECO Designer compares each logic cone in the design, determines which cones are different, and identifies only the changes needed to complete the ECO. The changes are highlighted by the green 'ECO' fragment in the new netlist shown in *Figure 3*. Only the necessary changes are made to a cone of logic.

Design teams are often challenged with ECOs that may be too complex to handle manually. In a post-mask flow, the ECO changes are mapped to available gates or freed gates. If insufficient resources are available, Conformal ECO Designer will inform the user. By only making needed changes to a cone of logic the amount of change to the physical design is limited. As demonstrated in *Figure 3*, reducing the amount of change required by the place-and-route tools minimizes the complexity and risk of the ECO.

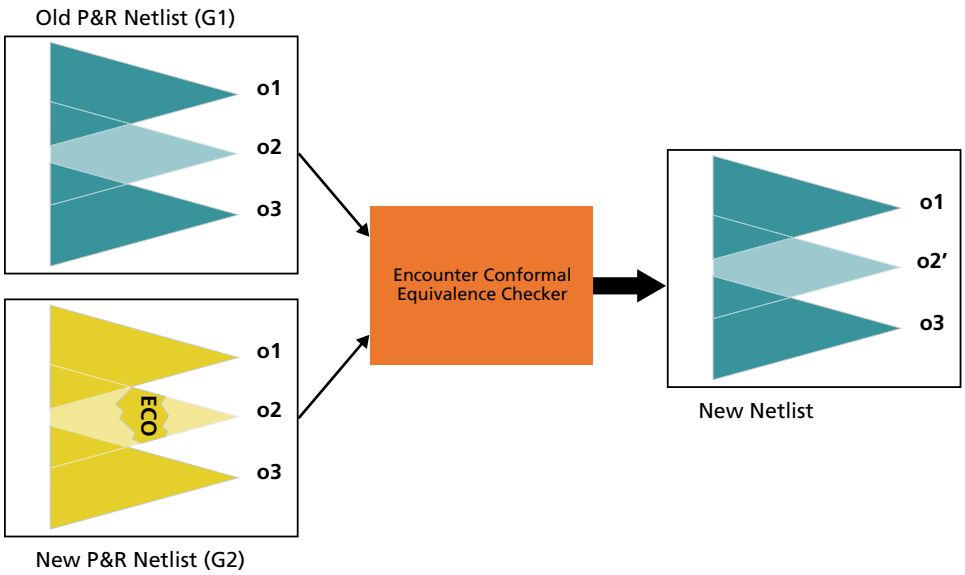

Figure 3: Conformal ECO Designer process diagram

A COMPLETE ECO SOLUTION

By enhancing the integration between Conformal ECO Designer and the Cadence SoC Encounter™ RTL-to-GDSII system, Cadence has created a complete ECO solution (*Figure 4*) that spans all parts of the design flow to achieve the highest quality ECO. Conformal ECO Designer performs feasibility analysis and implements the changes to the netlist if possible. Changes are then translated into physical implementation by the SoC Encounter System.

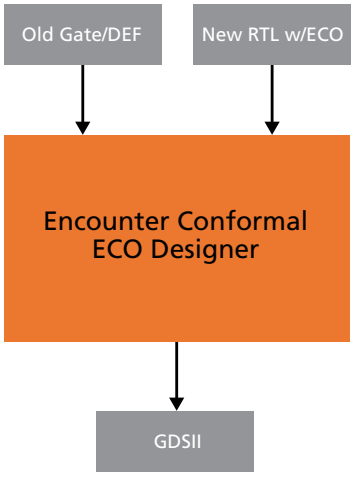

Figure 4: ECO framework

Conformal ECO Designer generates the modified logical netlist that is converted into the physical design. The conversion is handled by the SoC Encounter System, which has special features to process ECOs quickly and efficiently. The following paragraphs will highlight the capabilities of SoC Encounter.

The ECO flow, shown in *Figure 5*, starts with the Conformal ECO Designer. Conformal ECO Designer performs an analysis for post-mask designs to determine the feasibility of the ECO. If the ECO is not feasible, Conformal ECO Designer will indicate this to the user. The intent is to determine differences between the original netlist and the updated netlist. This provides information regarding the changes in the design. The changes are managed and merged with the original netlist to achieve the new logical netlist. The updated logical netlist is then passed to the SoC Encounter System for processing, which maps the changes to the physical netlist.

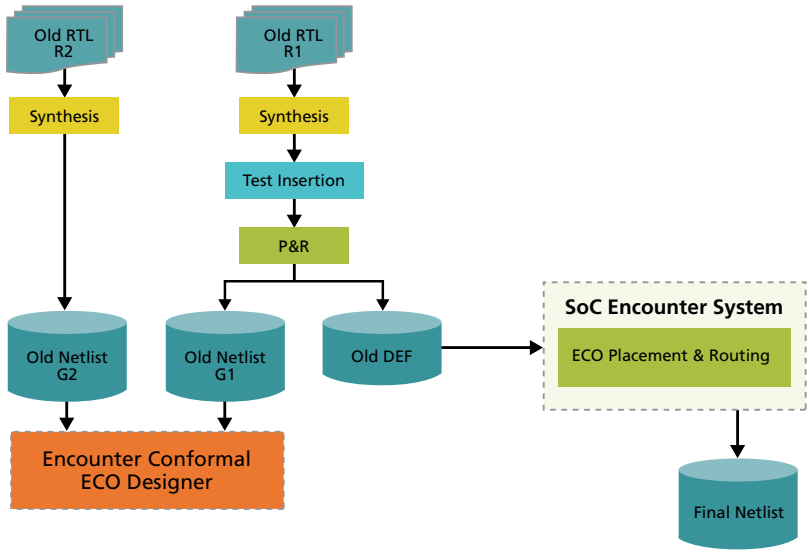

Figure 5: ECO Designer detailed flow

PLACE AND ROUTE

SoC Encounter System handles place and route. Within the SoC Encounter System there are several choices made depending on the state of manufacturing and cost savings that is desired. The most typical choices are pre- and post-mask ECOs. In pre-mask ECOs, designers can make changes by adding and removing gates, while at the same time minimizing changes to routing and existing placements. In post-mask ECOs, the changes made are based on spare gates or freed gates in the design. With post-mask ECOs, the goal is to preserve the base layers and only re-mask the metal layers. The post-mask ECO choices also apply to gate array cells, where the changes focus on the routing layers. Notably, SoC Encounter System will re-map the ECO to meet the physical design needs. It balances the needs of timing, design rule verification (DRV), and available spare gates to automatically optimize the ECO to the physical design.

SoC Encounter System also offers two sub-options for metal routing, shown in *Figure 6*. One is a complete mask change in which all metal layers are re-routed. The other is a limited mask change where only a few metal layers are processed, such as, for example, changing only a few metal layers (i.e., metals 1 to 3, in an 8-metal layer process). Reprocessing only a limited number of layers provides a significant cost savings over reprocessing all layers.

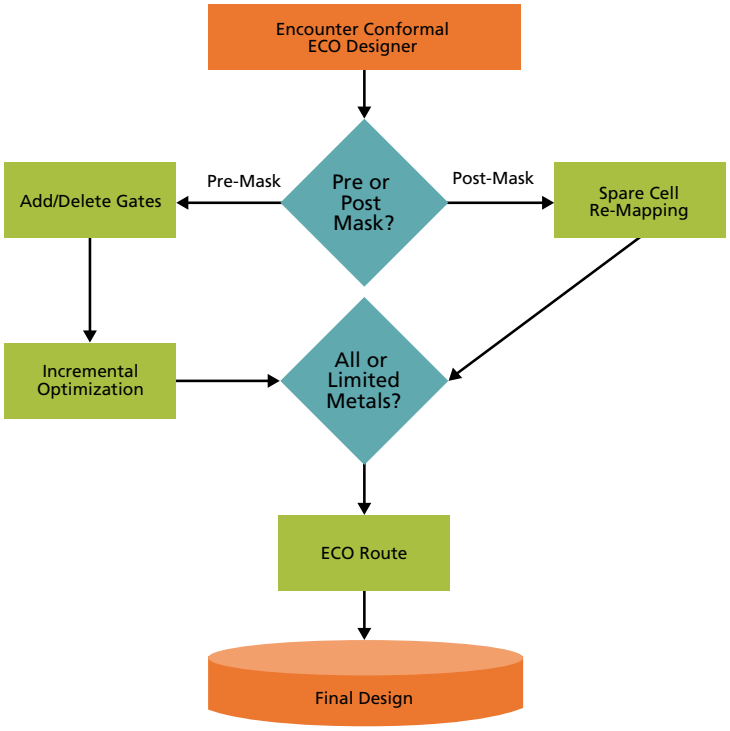

Figure 6: ECO routing decision tree

With SoC Encounter System, the design is physically remapped to meet the specific physical design requirements. As seen in *Figure 7*, a freshly imported ECO consists of spare cells, placed cells (untouched by the ECO), deleted cells (cells disconnected by the ECO), and new cells. Note, in this diagram the new cells have yet to be placed. The deleted cells are not actually deleted but preserved for post-mask ECOs to be used as possible spare cells.

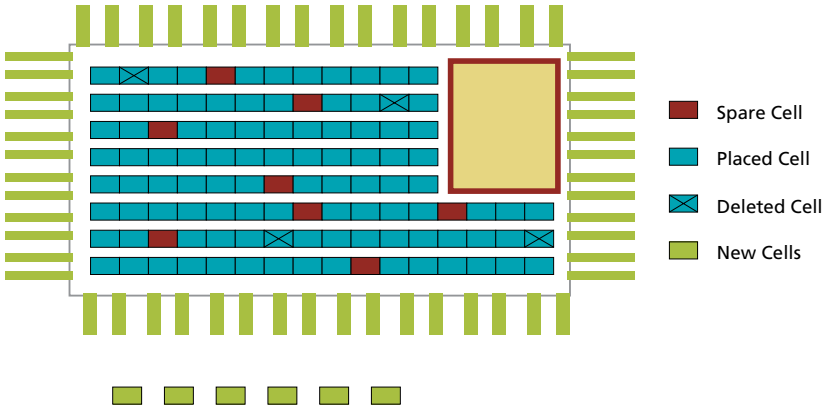

Figure 7: Design with ECO

When the design is physically remapped automatically, SoC Encounter System makes several decisions based on the function required, timing and DRV requirements, and the functions available in the spare cells and freed cells. For example, in *Figure 8*, a design requires a two-input 'NAND' gate. The only device available to meet the design requirements is a three-input 'AND' gate and an 'INVERTER'. SoC Encounter System will take advantage of those devices to meet the function and

the design requirements. This is a simplified version of the devices and functions that can be utilized. This now means ECOs are no longer limited to a one-to-one mapping of cells, **but to the availability of unused logic functions in the design.**

Figure 8: Physical remapping

As can be seen in the *Figure 9*, the new cells are functionally mapped into the design utilizing both spare cells and deleted cells. These are color-coded in the diagram according to the legend on the right. During remapping, SoC Encounter System will make the minimal number of changes. This includes minimizing route changes while connecting in new cells.

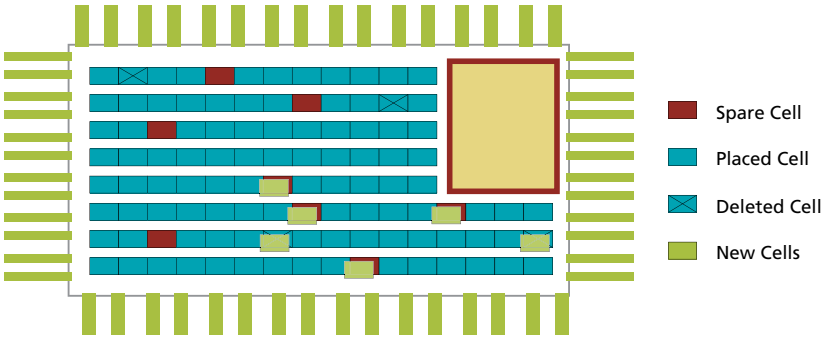

Figure 9: Design with ECO physically remapped

In addition, ECO Route can be limited to specific metal layers. By limiting the layer changes, SoC Encounter System can accomplish ECOs at greatly reduced cost. In *Figure 10*, the routing changes will be limited to metals 1 through 3 in a 5-layer process. The disconnected cell is broken off of *NetC* and the new spare cell is connected in metal 3 or below. All the while, the now disconnected upper metal layers are preserved to ensure the previously generated masks for the upper layers are preserved.

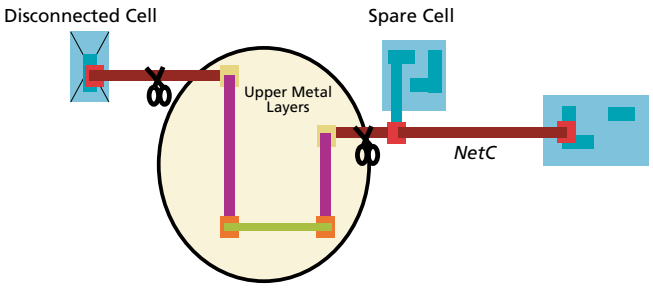

Figure 10: Limited layer ECO Route

SEQUENTIAL ECO

Functional ECOs can be further categorized into two types: combinatorial and sequential. Combinational changes are less involved and can usually be accomplished in metal layer changes (post-mask) if enough spare gates are available on the mask. Sequential changes are more involved and require rerunning of clock tree synthesis, and may also require fixing of scan chains. The steps involved in fixing scan chains depends on whether sequential elements were removed or added, and whether scan chains were broken. In the event spare sequential elements were already in scan chains, no breakage occurs. Similarly, sequential elements can be removed from the design and still remain in the scan chains with no breakage. The difficulty arises when new sequential elements are added (with no scan connections these then require incremental stitching). This capability exists with the synthesis technology of Conformal ECO Designer. As shown in *Figure 11*, the user can choose to make no changes to the scan or do incremental scan mapping and stitching. Once complete, the netlist is passed through to SoC Encounter System for processing to clean up the place and route. The last step in this flow is to pass the new scan setup and netlist to the ATPG solution for regeneration of the ATPG patterns.

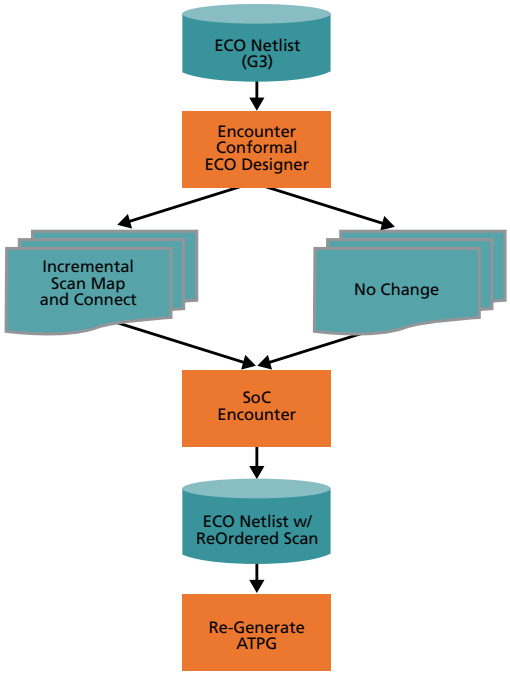

Figure 11: DFT in the ECO flow

CONCLUSION

With the high cost of generating and producing IC designs, all steps in the process are critical. When performing ECOs, mask costs alone can exceed a million dollars. The ability to limit mask changes to a few metal layers greatly reduces risk and cost. In addition, many ECOs are too complex to perform manually, which can limit an organization's ability to develop features sets and new products. Conformal ECO Designer, together with the SoC Encounter System, forms a complete Cadence ECO solution—from RTL to GDSII. Customers using the solution enjoy better predictability, faster process times, high-quality results, and lower costs, enabling design teams to process more ECOs to ensure products ship on time.

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