

## DO's and DON'Ts for Systematically Implementing Late Engineering Changes On Your Project

Project management and automation is quickly becoming the most critical element in the overall design and verification process. The key ingredients are good overall specification development that leverages planning with metric based checkpoints. The mentality of “beginning with the end in mind” allows for optimal resource usage, much higher design quality and realistic schedule estimates. Despite all the best planning, changes in requirements happen up to the last possible day.

Today's design teams typically do not address the problems that cause slips or productivity and quality issues. They tend to focus solely on individual tasks, engine performance, or languages, rather than defining the entire verification challenge, independent of its solution. In fact, most verification plans are merely a set of incomplete discussion notes that atrophy as the project moves forward.

Change management of the design and verification process needs to start with the goals of what needs to be verified. From this, an experienced verification team will have the ability to develop changes to the plan that are complete and inclusive of the intended goals.

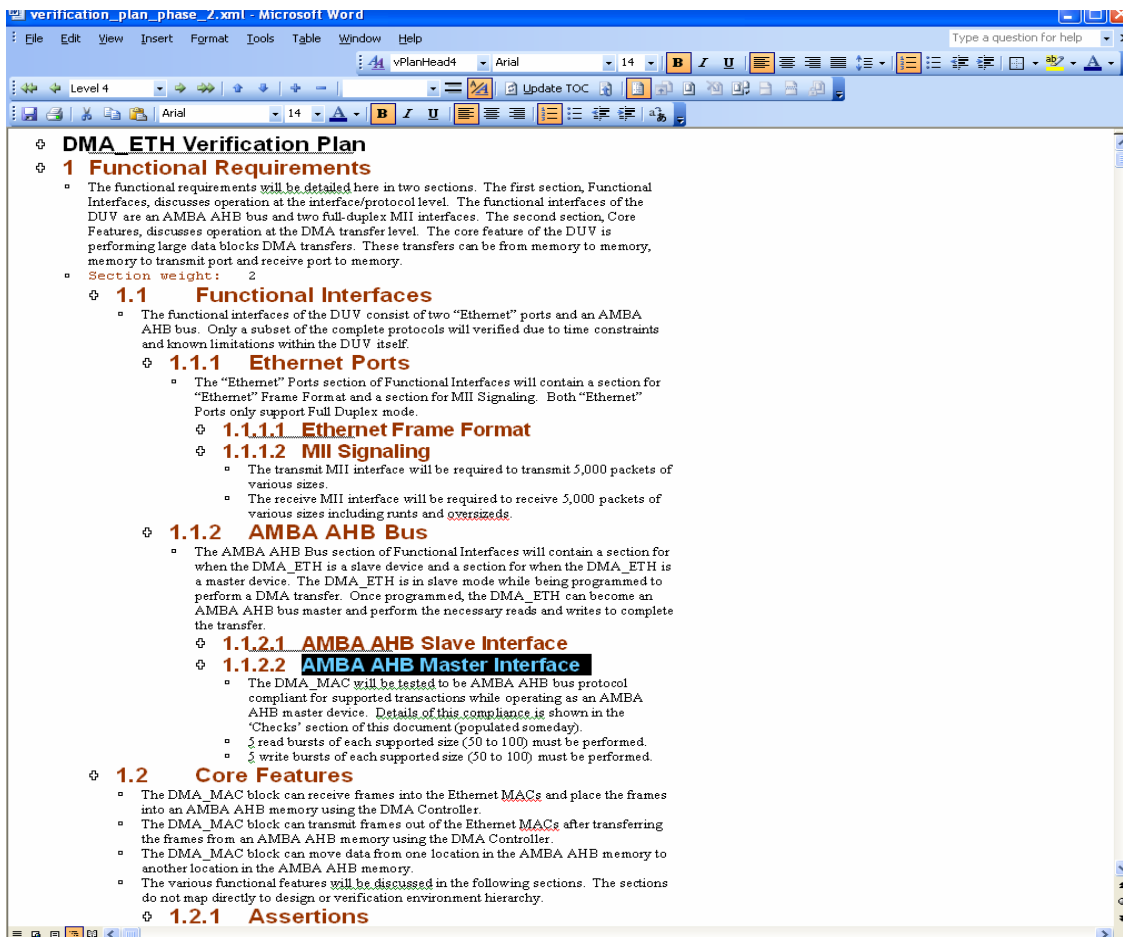


Figure 1: An example of a Verification Plan: which features we want to verify, by what date, by whom etc.

What is needed is a system that enables efficient introduction and tracking of changes as well as the right team approach to the required planning and implementation activities. Here are some of the basic do's and don't that you and your team needs to be aware of to introduce project changes effectively:

### Do's

- Must have a plan that is kept always up-to-date and is executable: your total coverage results after regressions will be mapped directly into your plan. This is used as the measure against which progress and completion is measured.

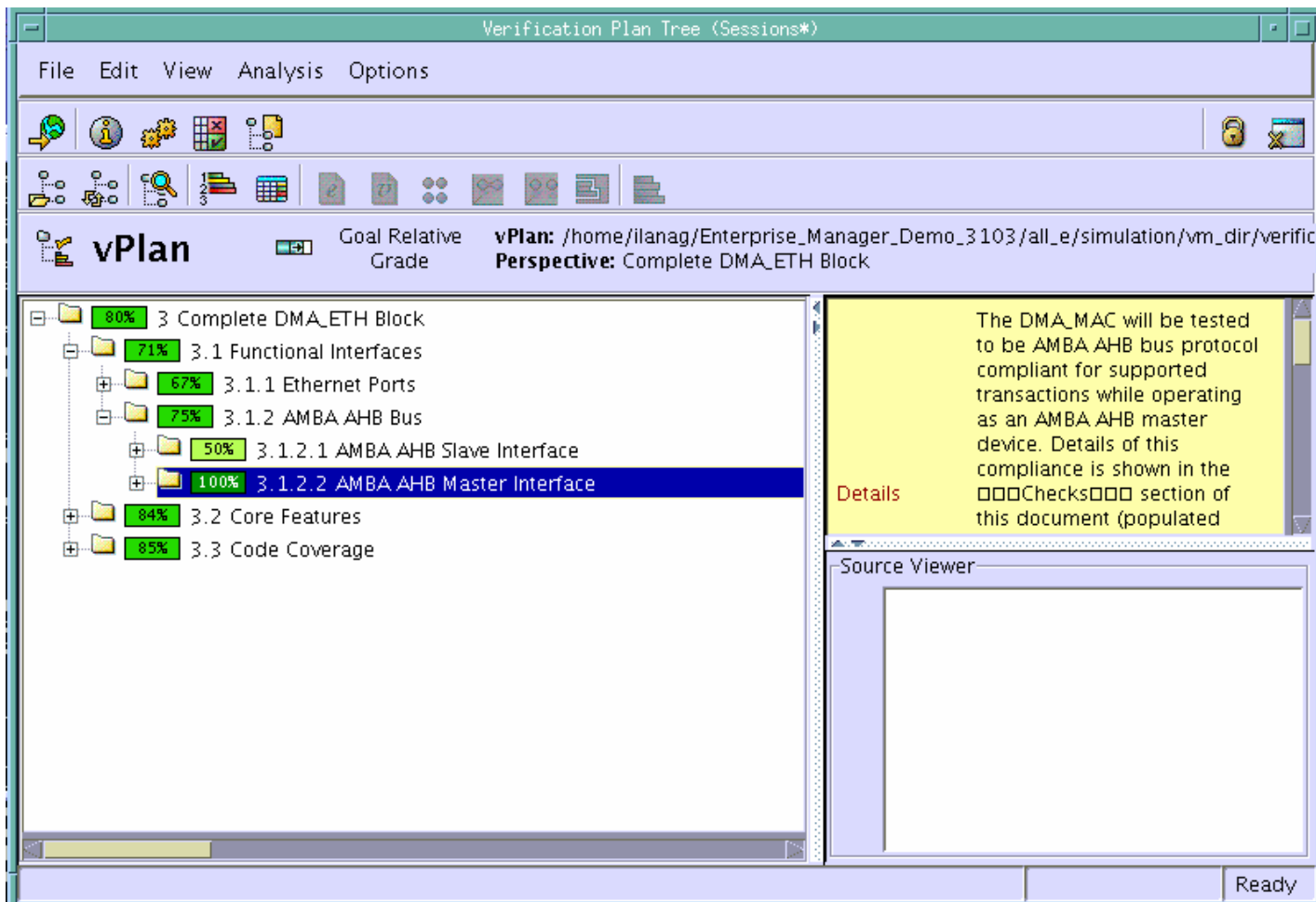


Figure 2: An executable plan – the coverage grades are mapped to the features in the plan

- You will need to identify all parts of the system that are impacted by each change and incorporate that into the overall plan before making any changes to the specification.
- Identify an owner of the change process that will be committed to following the process to completion. This person needs to have a good overall view of the project and maintain a high attention to detail.

- Measure the impact of changes by the scope of the change to the verification plan. Especially consider impact to various dependencies outside of your control -- such as any third-party cores; designs that may use third party soft or hard IP; or any dependencies on support from a semiconductor vendor.
- Review the effectiveness and quality of your process on a regular basis, and at the end of each project. Each change forced by errors in the past should be used as a learning experience and categorized for future projects.

**Only Slave In the AHB Interface**

**DMA\_ETH Verification Plan**

**1 Functional Requirements**

- The functional requirements will be detailed here in two sections. The first section, Functional Interfaces, discusses operation at the interface/protocol level. The functional interfaces of the DUV are an AMBA AHB bus and two full-duplex MII interfaces. The second section, Core Features, discusses operation at the DMA transfer level. The core feature of the DUV is performing large data blocks DMA transfers. These transfers can be from memory to memory, memory to transmit port and receive port to memory.
- Section weight: 2

**1.1 Functional Interfaces**

- The functional interfaces of the DUV consist of two "Ethernet" ports and an AMBA AHB bus. Only a subset of the complete protocols will be verified due to time constraints and known limitations within the DUV itself.
- **1.1.1 Ethernet Ports**
- **1.1.2 AMBA AHB Bus**
  - The AMBA AHB Bus section of Functional Interfaces will contain a section for when the DMA\_ETH is a slave device and a section for when the DMA\_ETH is a master device. The DMA\_ETH is in slave mode while being programmed to perform a DMA transfer. Once programmed, the DMA\_ETH can become an AMBA AHB bus master and perform the necessary reads and writes to complete the transfer.
  - **1.1.2.1 AMBA AHB Slave Interface**

**1.2 Core Features**

- The DMA\_MAC block can receive frames into the Ethernet MACs and place the frames into an AMBA AHB memory using the DMA Controller.
- The DMA\_MAC block can transmit frames out of the Ethernet MACs after transferring the frames from an AMBA AHB memory using the DMA Controller.
- The DMA\_MAC block can move data from one location in the AMBA AHB memory to another location in the AMBA AHB memory.
- The various functional features will be discussed in the following sections. The sections do not map directly to design or verification environment hierarchy.
- **1.2.1 Assertions**
  - Cover group: icc\_coverage.icc\_func\_hdl\_testbench.control
- **1.2.2 DMA Controller**

**2 Design Requirements**

- Section weight: 1
- **2.1 Code Coverage**
  - All module instances require code coverage
  - Cover group: icc\_coverage.\*.block
  - Cover group: icc\_coverage.\*.expression

**3 Verification Views**

- The verification perspectives are defined in terms of the coverage goal to be achieved by a particular date.
- **3.1 Complete DMA\_ETH Block**
  - This perspective includes all DMA\_ETH behavior in

**vPlan**

- 76% 3 Complete DMA\_ETH Block
  - 59% 3.1 Functional Interfaces
    - 67% 3.1.1 Ethernet Ports
    - 50% 3.1.2 AMBA AHB Bus
      - 50% 3.1.2.1 AMBA AHB Slave Interface
  - 84% 3.2 Core Features
  - 85% 3.3 Code Coverage

Figure 3: An example of a verification plan with an AHB interface and slave only – left. On the right – the executable plan that was created by reading in this verification plan

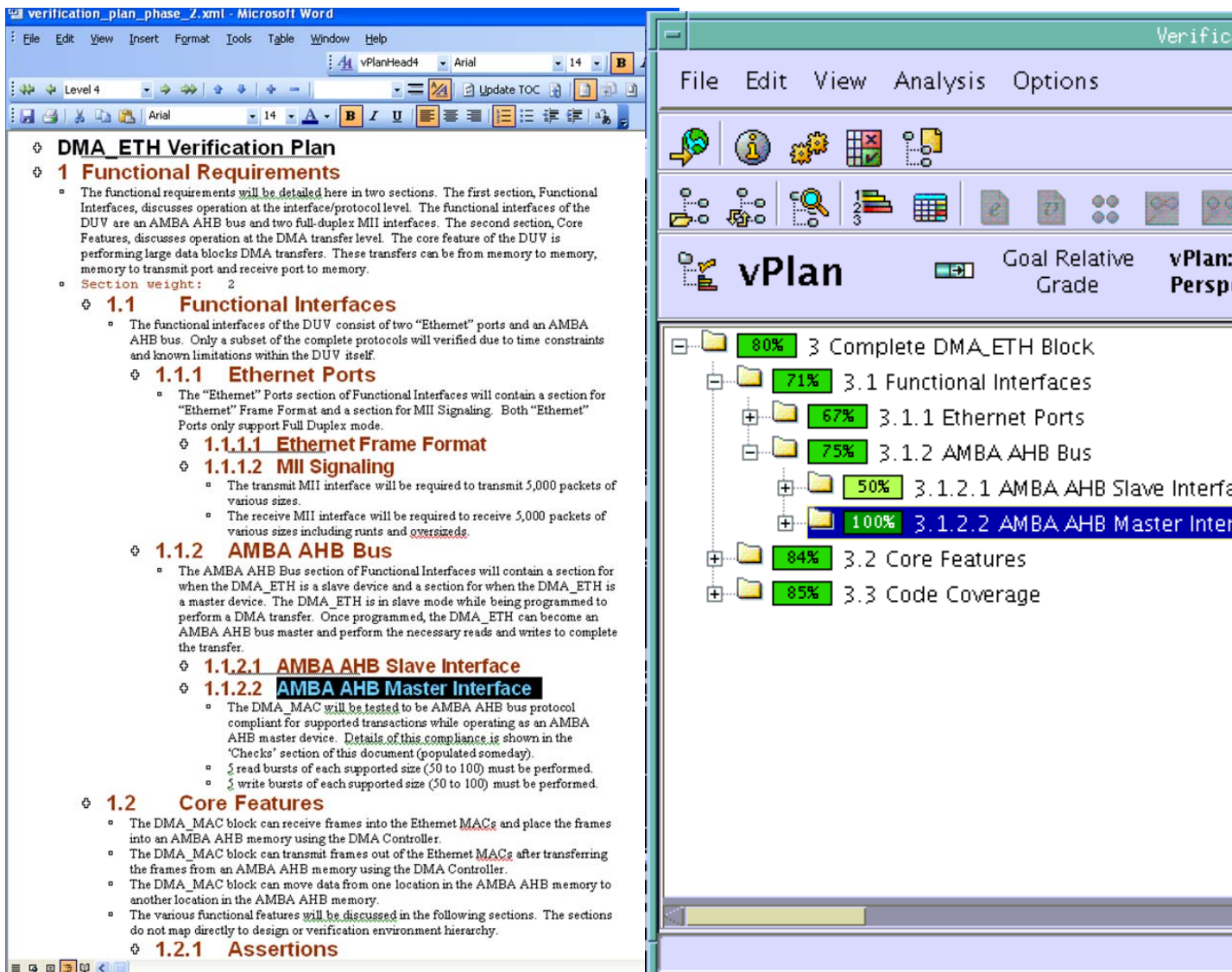


Figure 4: Lets assume that we want to add a master to the AHB Interface. We will first add it to our verification plan. The executable plan on the right shows the master added with its coverage grade after running the regressions.

## Don'ts

- Don't assume a change is completed until specific system behaviors exhibiting the change have been verified. Especially take care of changes up and down the entire process that reach far within other areas of specialization.
- Don't assume one person can implement a change to completion. Effectiveness in Verification is a lot higher with redundancy and cross-checks.
- Don't assume that a "simple change" is the best solution. At times, a simple change may create a "butterfly effect" and morph the system being verified from relatively stable to utterly chaotic. Watch out for the fallacy of simple solutions by reviewing changes with all adjacent groups and the architecture team.

- Avoid short cuts by not updating plans and all necessary metrics of quality. Short cuts may lesson quality, and often impact predictability as well as productivity.
- Don't change multiple parts of the system all at once without first assessing dependencies. In some cases, it may be prudent to verify the design in a few, well-defined iterations.

By following these simple guidelines, "good" planning based on verification management can be realized. Your organization will benefit as all stakeholders begin to leverage the ability to capture and review the verification plan as you drive you next design to closure.

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