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Low Power Methodology on a Multicore Networking chip

Udupi Harisharan (Cisco)

Kanakalakshmi Ranganathan (Cadence)

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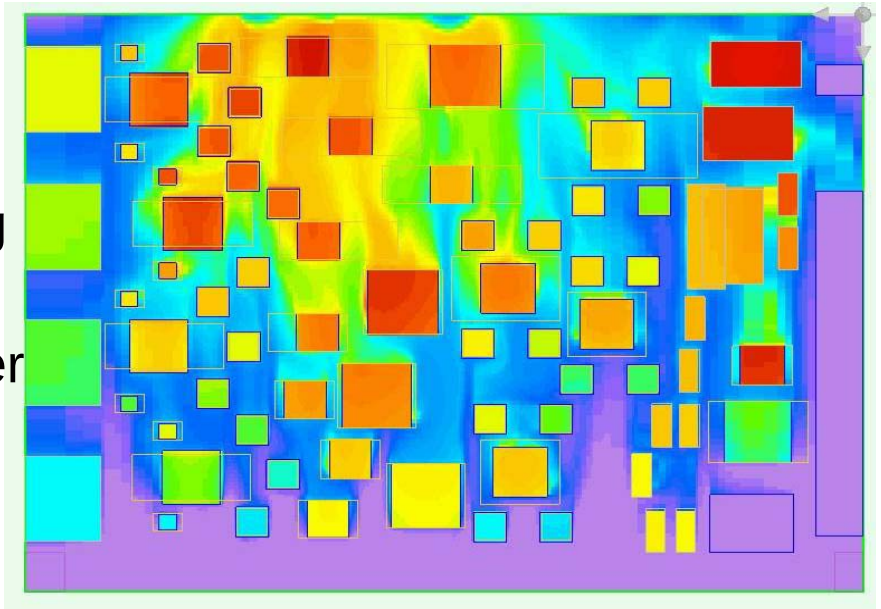
Motivation

- Power is a limiting Factor in System Design
  - Average Power Dissipation
  - Peak Power Dissipation
- Peak Power a key concern in Line Powered Systems
  - Thermal Dissipation in the system
  - Reliability Issues

Thermal Limitation

- Multi 100GBit Throughput line cards
  - Similar Form Factors as Previous generation Systems
  - High Power Densities

- Issues
  - High Junction Temperatures
  - High Cooling Costs and challenging Power delivery
  - Expensive Real estate in Datacenter



Asic Power

- ASICs consume more than 50% of Board Power budget
- The Asics are typically “Always On”
  - Dynamic Power
- Different units in the Chip operate at Different speeds or Processing capacity

Power Saving Options

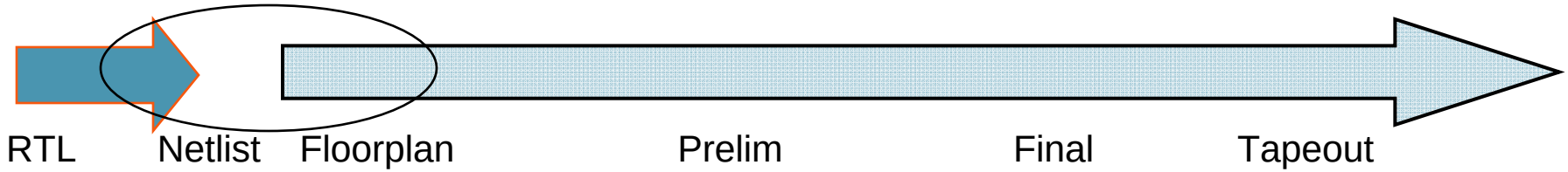
- Voltage Islands
  - "Always on" Multiple Voltage partitions in the Chip
  - Partitions connected through Level Shifters
  - Helps save Peak Power
  - Helps save Dynamic (square) and Leakage Power (cubic)
- Clock Gating
  - Gate the flops with no Data Transition
  - Helps save Average Dynamic Power

Voltage Island Partitioning

- Voltage Island Partitions – Power vs Performance
- Based on Frequency - if Clear Clock domain separation Exists
- Multi-VDD Exploration of the Logical partitions

ASIC Design Process – Multi-VDD

- Need to have Initial Partition Ready by Floorplan Handoff Stage



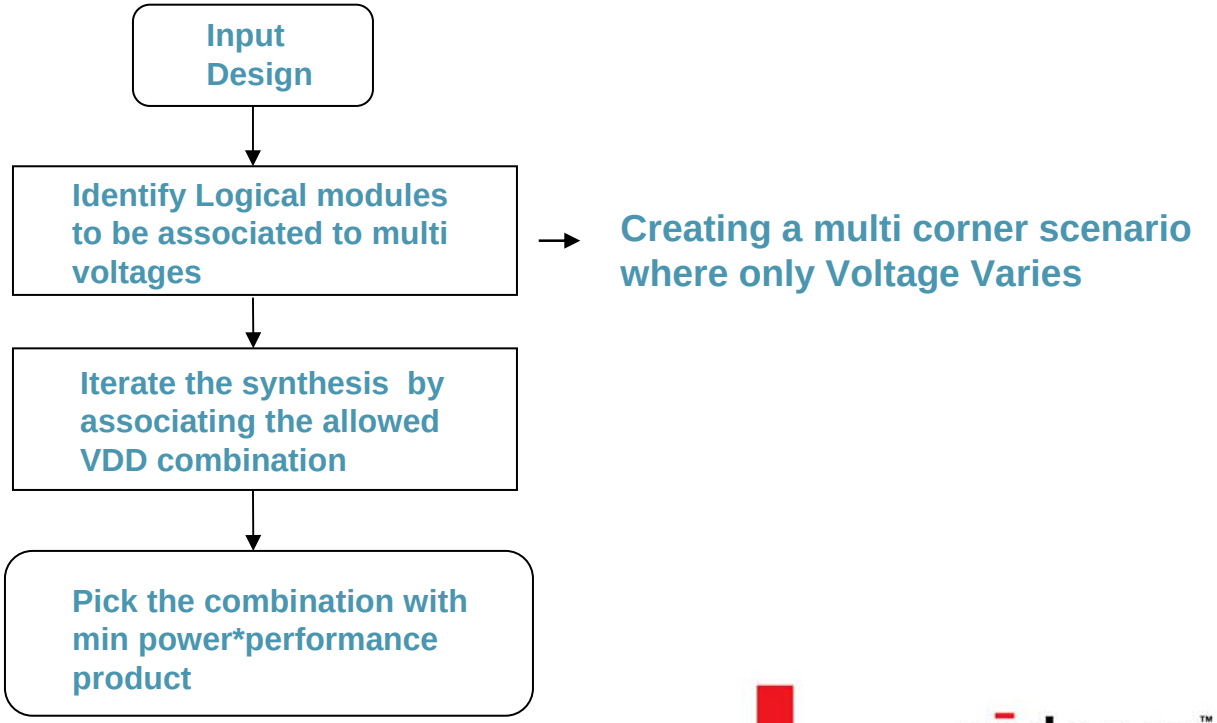
- Need to have Early Exploration Mechanism

Requirements

- Need early Multi-Vdd Partition Exploration Capabilities
- Need to measure Timing and Power simultaneously
- Exploration method should have Good correlation to Layout

Exploration Flow

- Power-Performance Product –
  - RequiredTime*Power



Power Saving Exploration – Test Case

- The Flow described can be extended to take Advantage of different Process and Vdd options.
- Used Unit Processor for the Test Case
- Has a combination of Low Power and General Purpose Libraries
- LP - 1.2V and GP - 1.0V
- Worst Case PVT for Power
  - Fast,Vdd+10%,HighT(125)degC

RTL Compiler – Multi-VDD (What-if analysis)

- What-if analysis was implemented by dynamically changing the library domains to the modules in a single RC session
- RC's library mapping features where used to simultaneous consider slow corner timing and fast leakage corner for power optimization and reporting
- Top down Multi-vt optimization was also enabled for Leakage power optimization.
- Once the best scenario was identified a CPF (Common power format) file was generated to be used across the implementation tool to pass on the power constraints.

RTL Compiler – Multi-VDD

- Results Explored Post Map stage
- Scenario 3 has the Lowest Power*Performance

	Scenario1	Scenario2	Scenario3	Scenario4	Scenario5	Scenario6	Scenario7	Scenario8
Top	1.0V	1.0V	1.0V	1.0V	1.0V	1.0V	1.0V	1.0V
Execution	1.2V	1.0V	1.2V	1.0V	1.2V	1.0V	1.2V	1.0V
Instruction	1.2V	1.2V	1.2V	1.2V	1.0V	1.0V	1.0V	1.0V
Register	1.2V	1.2V	1.0V	1.0V	1.2V	1.2V	1.0V	1.0V
Area (um2)	***158053***	***160257***	***154964***	***124056***	***154250***	***154674***	***149402***	***113078***
Instances	12657	17717	12864	10384	12006	17080	12136	8540
Levelshifter	2981	2778	3004	805	2436	2094	2341	0
Timing Goal (ps)	1000	1000	1000	1000	1000	1000	1000	1000
Slack	126	104	127	90	144	160	144	158
RequiredTime (ps)	***874***	***896***	***873***	***910***	***856***	***840***	***856***	***842***
Power Dyn (nw)	39123202	37150445	33329476	31927467	38689083	38013054	32923774	31461703
Power Leak (nw)	9008434	15904439	11992645	30660406	18226651	25805942	21346728	39596345
Total Power (nw)	***48131636***	***53054884***	***45322121***	***62587873***	***56915734***	***63818996***	***54270502***	***71058048***
Required Time * Power	420.6704986	475.3718	***395.6621***	569.5496	487.1987	536.0796	464.5555	598.3088

Multi-VDD Exploration

- As an example we Save about 36% power in scenario3 vs no Multi-VDD (all 1.0V)
- Explore the Timing and Power simultaneously
- Synthesis Based Sequential Multi-voltage Approach described

Conclusions and Recommendations

- Early Exploration of Multi-VDD partitions Necessary
- Expand the methodology to predict QOS
- Need to Validate the Exploration Results Post Layout

Appendix 1

- Exploration Scripts :

RTL Compiler Synthesis scripts

Common Power Format (CPF) script

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