Low power verification flow to ease the pain in implementing MTCMOS based MSMV wireless design

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ABSTRACT

Power management on chips has become a critical design factor. Designers reduce dynamic and leakage power consumption of mobile and wireless devices by employing various techniques during the design implementation phase. The power dimension to design closure presents significant new challenges besides the usual concerns over design functionality, performance, and die size. All designs at 65nm and beyond will utilize techniques such as state retention flops, multiple voltage and power domains, MTCMOS switch and DVFS. These techniques increase design complexity and elevate the risk of an implementation mistake. For example, the use of multiple voltage domains requires that signals crossing the voltage domain boundaries be level-shifted appropriately. The use of power domains in power-sensitive designs requires that certain signals be isolated correctly under the power-down condition. The presence of multiple voltage and power domains leads to complex power and ground connectivity issues on the chip that need to be checked. The EDA tools for implementing and verifying these techniques are still evolving. Implementation mistakes caught by late-stage power and ground rail-aware simulations that take the design back to the synthesis stage, can cost months. With the flow proposed in this paper, such bugs can be expeditiously identified and resolved.

Key Terms – POWER GATING, MTCMOS, MSMV, SRPG

I. INTRODUCTION

Power management has become critical in the design of wireless and handheld devices. Power consumed by a chip significantly influences its packaging and is a key determinant of the cooling requirement for large electronic systems. Reduced talk time on cellular phones negatively impacts both consumers and wireless service providers.

This section describes the prevailing low power terminology, source of power dissipation in a CMOS design and some ways to mitigate the power loss. A CMOS design consumes power during Functional, Idle, Power-down and Test modes. During the functional mode, the chip runs at the target speed performing its primary function. In the Idle mode it runs at reduced voltage or frequency and performs an abbreviated set of activities. In the Idle mode, often there is no activity in parts of the chip. In the Power-down mode, certain selected logic blocks are switched off. Operation of the low power chip in test mode also presents unique challenges. Exceeding the power rating of the chip during the manufacturing testing can damage the gate oxide and potentially destroy the chip. Similarly, powering on or off several IP blocks simultaneously on an SOC can cause a current surge.

The total power dissipated in a CMOS device is the sum of dynamic and leakage power. The two components of the dynamic power are: transient short circuit power and internal capacitance charge-discharge power. The fundamental equation to represent the dynamic power is:

$$\mathbf{P_{dynamic} = A\, C_L V_{dd}^2 f}$$

where **A** is the switching activity factor, $\mathbf{V_{dd}}$ is the supply voltage, $\mathbf{C_L}$ is the load capacitance that is charged or discharged and **f** is the clock frequency.

Leakage power is the static power that is dissipated during Functional, Idle and Power-down modes. The leakage power is a function of design and device parameters.

$$\mathbf{P_{leakage} = f\,(Vdd,\, V_t,\, W/L).}$$

One of the most effective ways to minimize dynamic power is to scale down the voltage, since power has a quadratic dependence on voltage. However, lowering the supply voltage increases the propagation delay, reduces the performance of the chip and worsens susceptibility to noise. Insertion of additional pipeline stages may be required to maintain the design bandwidth. Using low $\mathbf{V_t}$ cells to meet aggressive timing goals exacerbates the leakage power problem. Below 65nm sub-threshold current and gate oxide leakage current contribute significantly to the overall power. Since voltage scaling alone is no longer adequate to manage power dissipation of a chip, designers resort to Power Gating and multiple supply multiple voltage (**MSMV**) techniques to minimize leakage power.

The best way to reduce power is to shut it off completely. During **Power Gating** the power to a module or a cell can be turned off or on. This is accomplished by using Multi-threshold CMOS (**MTCMOS**) switches that connect the external power or ground rail to the local power or ground rail. A high threshold (i.e. low leakage) sleep transistor connects the power or ground mesh of the low threshold i.e. faster transistor logic blocks to the external power or ground mesh. Depending upon the requirements, a designer may choose a header or a footer MTCMOS cell. In a coarse-grained configuration, the MTCMOS switch can be used to turn off an entire power domain. A power domain is a group of logic that shares the same power net. In a fine-grained

configuration, the MTCMOS switches can be placed inside cells and can be distributed throughout the design.

The addition of MTCMOS cells makes the design more susceptible to wake up latency, ground bounce and area congestion. To expedite the wake up sequence of the power gated logic, the state values of the logic block prior to being shut down are stored in State Retention Power Gating (**SRPG**) cells. An SRPG cell is a special type of D flip flop whose master latch runs on a switchable power and the slave latch runs on a continuous power. Special circuitry enables an SRPG cell to retain the state of the system prior to the power shut off and restores the prior state after a power up sequence. The state of the system could also be stored and retrieved from an external memory. Such a design would add extra latency to the wake up sequence.

A low power multiple supply voltage design (MSV) can either be multiple supply single voltage (MSSV) or multiple supply multiple voltage (MSMV). In an MSSV design all of the logic blocks have the same voltage but independent supply rails. In an MSMV design different blocks operate at different voltage levels. Two logic blocks that have the same supply voltage magnitude are said to be in same voltage domain. In this paper two logic blocks that have the same voltage values could be in different power domains if they do not share the same power net.

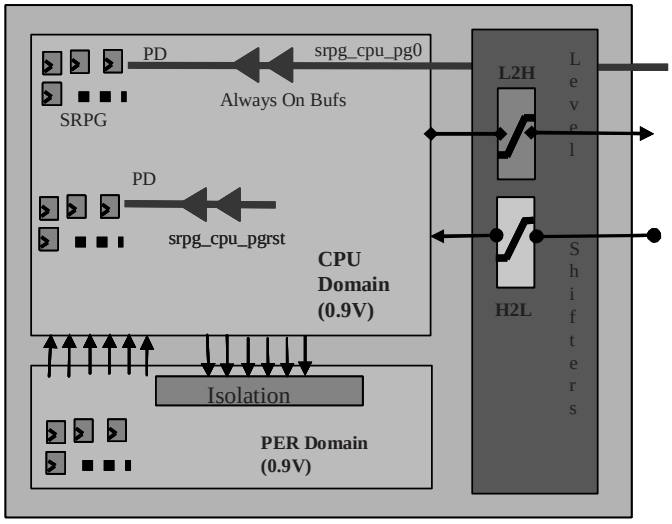
The rest of the paper will describe the following: Section II summarizes the architecture of the design that implemented the aforementioned techniques. Section III discusses common errors that occur in such an implementation and how no other flow can catch them. Section IV describes a few real errors caught by this flow, and Section V outlines the scope for future work.

II. ARCHITECTURE OF THE DESIGN

This low power design consists of two main power domains – a CPU domain and a peripheral domain, both operating at 0.9V. These domains are further embedded in an SOC, operating at 1.1V. The level shifters are inserted on all the signals crossing from the 0.9V domain to the 1.1V domain. Both CPU and peripheral domains can be switched off independently. The MTCMOS switches are placed at the boundary, in the SOC domain. The level shifters used in the design also have built-in isolation which isolates the outputs going to the SOC domain. The valid shut down modes are:

1) Both CPU and peripheral domains are off
2) CPU domain is off but the peripheral domain is on

These low power modes require isolation cells at the boundary crossing between the CPU and peripheral domain. There is no need to isolate signal crossings from the peripheral to the CPU domain as there is no mode in which the peripheral domain is off and the CPU domain is on. The flip-flops in the CPU and peripheral domain are SRPG flops, which save design state during the power down mode. All the low power control signals (e.g. power-down and isolation control) are buffered using Always-On (AON) buffers. It was absolutely critical for success of this design to have all of the foregoing features implemented correctly. A single mistake in implementing the power domains or the control signals that managed them could have been fatal to the design.



III. COMMON IMPLEMENTATION ERRORS IN LOW POWER FLOWS

Both MSMV and Power Gating techniques reduce dynamic and leakage power at the expense of added design and verification complexity. The MSMV flow requires the insertion of level shifters in a design. The Power Gating technique necessitates adding MTCMOS switches, SPRG cells, isolation cells and Always-On logic in the design. The resultant design poses new verification challenges and is prone to some of the common implementation errors that are described later in this paper. RTL languages lack low power constructs and unless explicitly instantiated do not support low power structures. Formal verification of the logical functions of the power controller at the RTL level, while useful, is by no means complete. Low power functionality is considered complete only after the design has been placed and routed. Gate level simulation is time prohibitive and does not provide sufficient verification coverage. Here are some of the common implementation errors that occur in a low power design:

1) Level Shifter Cells

A level shifter in an MSMV design transports a signal from one voltage level to another. The output of the level shifter could be higher or lower than its input voltage. Missing level shifters, redundant level shifters, level shifters with incorrect direction or power connectivity are some of the common verification errors seen in an MSMV design.

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2) SRPG Cells

An SRPG cell saves the state of the design prior to shut down and restores the state of the design after the wakeup sequence. Some of the hard to detect implementation mistakes involving SRPG cells are: a power pin of a state retaining slave latch connected to a switched power supply, a retention signal coming from a domain whose power can be turned off, a retention instance control pin with the wrong polarity or a retention cell control pin unconnected to a user specified control signal. While the preceding list of potential errors is by no means exhaustive, any one of them could cause the system to lose state and malfunction. Structural checking of SRPG cells alone is not sufficient. Using formal verification, the functionality of SRPG cells needs to be verified. For example, property checking can conclusively prove that whenever the retention signal is asserted or de-asserted, the local clock to the SRPG cell is disabled. This reduces power dissipation and ensures the correct sleep and wake up sequence of the SRPG cells.

3) Isolation Cells

Floating input on a CMOS device can simultaneously turn on both the PMOS and NMOS transistor stacks. The resulting short circuit current can potentially destroy the device. Therefore any signal that originates in the shutdown domain and drives a logic gate in the powered on domain must be properly isolated. Some of the common errors seen in designs with Power Gating are: missing isolation cells, redundant isolation cells, invalid isolation cell type, wrong isolation cell location and isolation cells with wrong isolation control or floating outputs.

As in the case of SRPG cells, structural checking of the isolation logic while necessary, is not sufficient to guarantee the correct low power behavior of the design. Formal verification should be used to verify that the power controller in the design is generating the correct isolation signal. This static verification technique does not require the user to write test vectors or explicit assertions.

In addition to the common errors described in the preceding sections, the verification methodology must check for correct power and ground pin connections for power switches and Always-On cells. The verification flow must ensure that only AON cells are placed in the path of the retention and isolation signal.

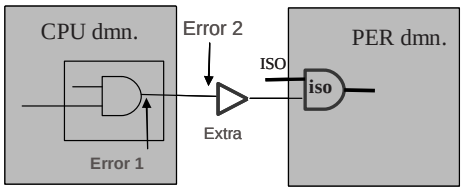
IV. ACTUAL ERRORS FOUND BY THIS FLOW

The Conformal Low Power product from Cadence Design Systems, Inc. was used to verify the correctness at each stage of the implementation flow, including synthesis, scan insertion, place & route (P&R), clock tree synthesis and high fanout synthesis, and during optimization at different phases of the design flow. This approach detected bugs early and prevented costly late stage ECO changes. A gate level Verilog netlist was used for checks at the Synthesis stage. A "physical" Verilog netlist (i.e. gate level Verilog netlist with power and ground connectivity) was checked after the design was placed & routed. The following are key representative errors found during the different phases of the design flow.

A. Logical netlist errors:

1. Error 1&2:

In this example the synthesis tool inserted an extra buffer before an isolation cell. This causes an error for the missing isolation cell at the CPU domain boundary and another error for the top level buffer input coming from a shut down domain without isolation logic.



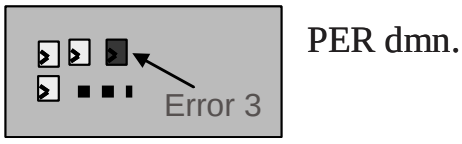
Error Messages:

ISO7: Missing isolation cell
Severity: Error Occurrence: 6
Missing isolation cell at 'arm11p_per_domain/…/GTECH_ISO1_EN0_nex_aipsa_rdata_32_1_7/U310_OR/A' (domain VDD_PER_ISO) from 'arm11p_cpu_domain/arm11p_cpu_core/ahb_nex_top/U19239/Z' (domain VDD_CPU)

ISO7: Missing isolation cell
Severity: Error
Missing isolation cell at 'arm11p_per_domain/…/GTECH_ISO1_EN0_nex_aipsa_rdata_32_1_6/BFX_HS65_*_BFX4/A' (domain VDD_PER_ISO) from 'arm11p_cpu_domain/arm11p_cpu_core/ahb_nex_top/U19237/Z' (domain VDD_CPU)

2. Error 3:

In this example one of the flops in the shut down domain was synthesized as a non SRPG flop

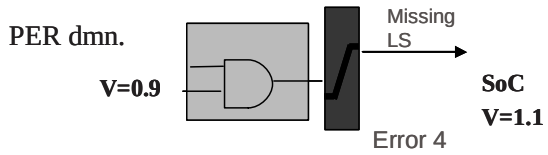


Error Message

RETRULE1.4: Instance not mapped to retention cell 'arm11p_per_domain/arm11p_per_modules/*_term_sel_reg/U$1' is not a retention instance (retention rule SRPG_rule2)

3. Error 4:

In this example one of the outputs going from the peripheral domain to the SOC domain was missing a level shifter



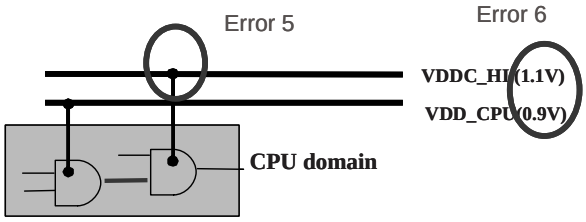
Error Message

Missing level shifter at 'arm11p_lvl_shift/arm11p_lshift_ wrapper/lshift_per_domain/lshift_lh_ipsa_wdata_21/BFX_H D65_*_BFX36/A' (domain VDD_LSHIFT3, voltage 1.1V) from 'arm11p_per_domain/arm11p_per_test/arm11p_per_wrapper/ U6281/Z' (domain VDD_PER, voltage 0.9V)

B. Physical netlist errors:

4. Error 5 & 6:

In this example the P&R tool connected the logic in the CPU domain to L1 memory array supply (1.1V). This caused two types of errors. - one for the wrong power connection and another one for a 0.9V cell being connected to the 1.1V supply without a level shifter.



Error Messages:

ISO7: Missing isolation cell
Severity: Error Occurrence: 6
Missing isolation cell at ‘arm11_cpu_domain/ …/TOP2188/A' (power domain VDDC_HI) Driver is ‘arm11_cpu_domain/…/U15827/Z' (power domain /vdd_cpu)

Missing level shifter at ‘arm11_cpu_domain/…/TOP2188/A' (domain VDDC_HI, voltage 1.1V) from ‘arm11_cpu_domain/ …/U15827/Z' (domain /vdd_cpu, voltage 0.9V)

5. Error 7:

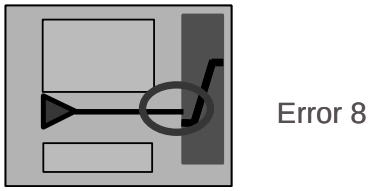
In this example one of the buffers added during optimization stage was not connected to the power rails.

Error Messages:

PDM4d: Power pin of a library cell is not connected to a power net
Power pin 'vdd' of instance 'arm11_cpu_domain/TOP128' (module HS65_*_BFX40) is not connected to a power net

6. Error 8:

In this example one of the cells was placed at the top level and thus did not belong to any power domain. This resulted in a level shifter being connected to a cell with no clear power domain on one side.

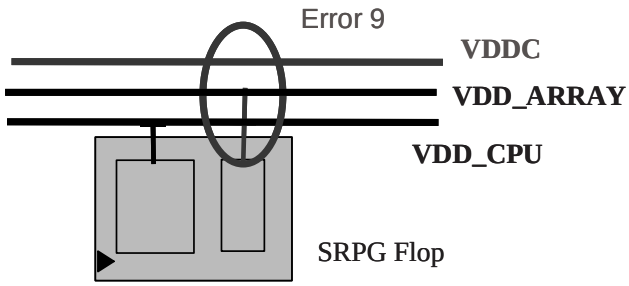


Error Messages:

LSH1.1: Input connected to an incorrect voltage
Severity: Error Occurrence: 93
Pin 'A' of 'arm11p_lvl_shift/…/level_shifter' (module HS65_*_LS_L2HIHX31) is connected to Mixed Power Domain
Expected voltage domain is 0.9V
Pin driver is ‘arm11_cpu_domain/…/TOP1812/Z‘

7. Error 9:

This example shows that the retention latch of a SRPG flop was connected to a switched supply instead of an Always-On supply VDDC.



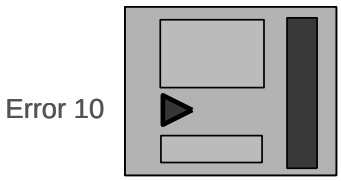
Error Messages:

RET1: State retention cell retention power can be OFF when normal power is ON
Severity: Error Occurrence: 1

Instance:
arm11_cpu_domain/…/_dc_mem_q_pip_r_reg_8_
(HS65_*_SDFPRQNX4_SRPG)

8. Error 10:

In this example one of the cells was placed at the top level and thus did not belong to any power domain.

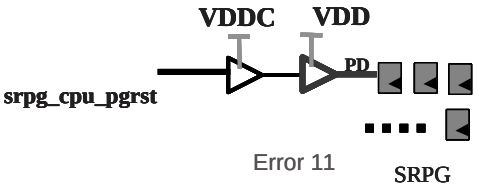


Error Messages:

PDM1: Power domain of the instance is unknown
Severity: Error Occurrence: 2
Instance name: arm11_cpu_domain/…/TOP1812
Module name: HS65_*_OR2X4

9. Error 11:

Switched power supply was connected to one of the buffers on the path of the power down control signal for an SRPG cell. This control signal can never shut down so it was expected to be powered with Always-On buffers only.



Error Messages:

AON1: Power pin of always-on instance can be off while its load is on
Severity: Error
Instance: arm11_cpu_domain/../ARM11P_ALWAYS_
ON_NET__G1B1I1_16ASTttcNet30413 (HS65_*_IVX40_
VDDC)
Power pin vddc is connected to power switch '/vdd_cpu'

V. FUTURE WORK

The advanced power management techniques described earlier in this paper cannot be easily implemented at the RTL level. In general, the notion of power switches, isolation logic, SRPG cells, and Level shifters does not exist in the RTL domain. These low power structures are added to the design during Synthesis and Place & Route. This creates a chasm in the design and implementation flow since RTL can no longer be considered golden and cannot be compared to the final design netlist.

Common Power Format (CPF) provides support for all design and technology related power intent information to be captured in a single ASCII text file that can be used throughout the RTL to GDSII flow including simulation, formal verification, synthesis, test, physical implementation and sign off analysis.

VI. ACKNOWLEDGEMENT

Authors thank Harish Ananthamurthy and Mitchell Hines of Cadence Design Systems, Inc. and Anuj Singhania of Freescale Semiconductor for their technical insight and excellent support during all stages of the verification flow.

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