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# Automating Functional ECOs using Encounter Conformal Technology

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# Agenda

- About AMD
- About **Group CAD SAPR**
- Existing ASIC Flow Described
  - **SAPR**
- ECO Challenges for SAPR Flow
- Conformal ECO Put-to-the-Test (& Results)
- ECO Flow: Integrating Conformal ECO
  - **Incr-SAPR**
- Summary
- Benefits

## About AMD

***From then... 1969:*** "... AMD incorporates with \$100,000; establishes headquarters in Sunnyvale, California."

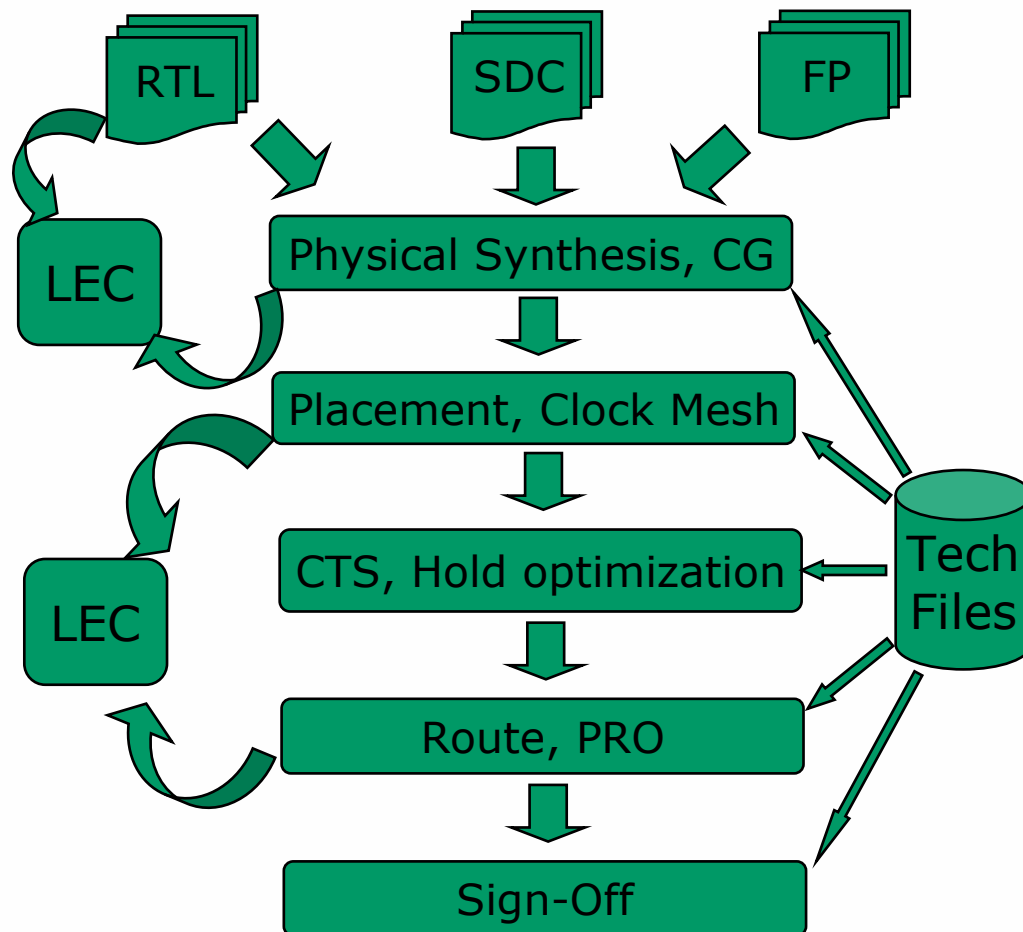
***To now... 2007:*** "... Over the course of AMD's three decades in business, **silicon and software** have become the **steel and plastic** of the worldwide digital economy."

***Today...*** AMD is a **customer-centric** innovation company, a processing powerhouse that offers **smarter choices** for its customers and makes technology more accessible to the world.

## About SAPR CAD group

The Synthesis Auto Place & Route (SAPR) expert group addresses the digital design flow requirements

# AMDs 45nm SAPR Design Flow

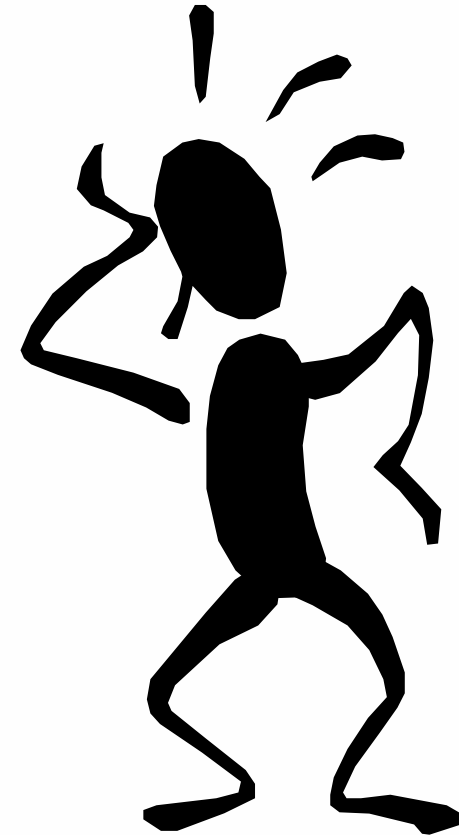
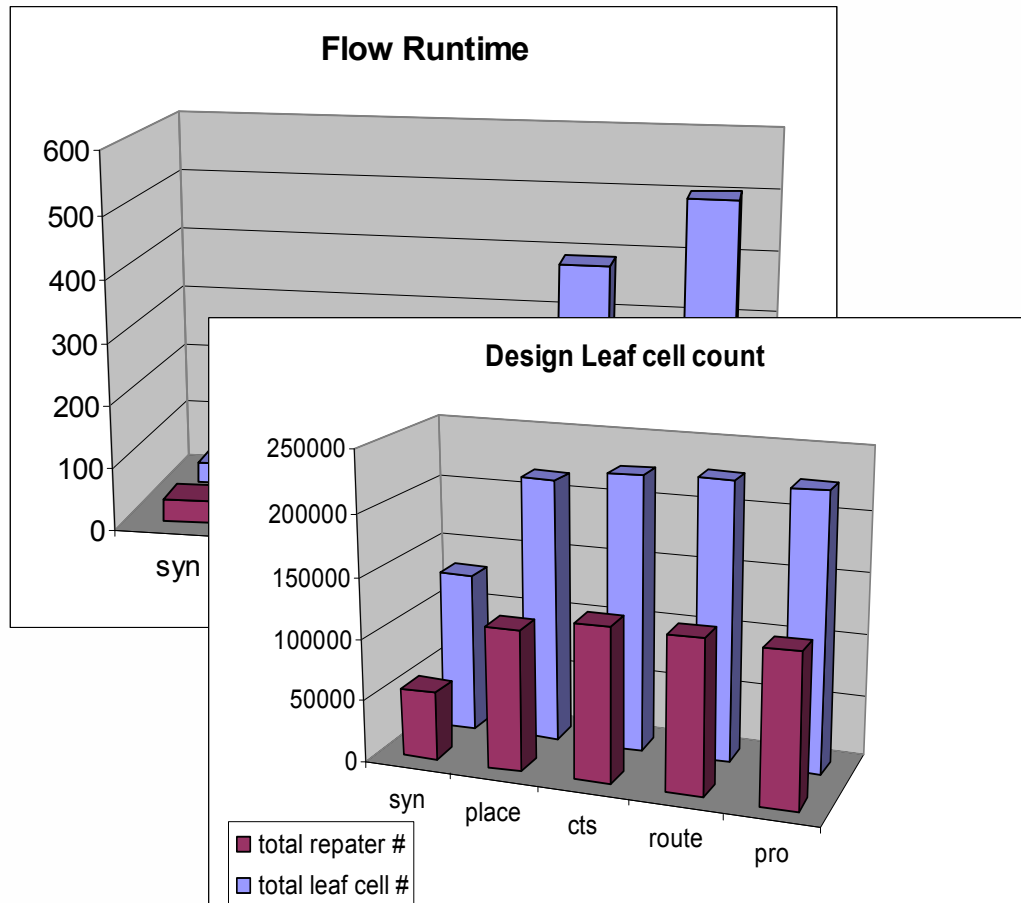


- Synthesis + Auto P&R
- Block Size:  
250-500k instances
- SAPR Cycle:  
~1-4 days
- Timing:  
Up to 1GHz  
Up to 8 clocks

# Common SAPR Design Challenges

- Design Performance  
Timing, Area
- Design Power  
Leakage, Dynamic Power
- Design Cycles  
Time to Market, Implementation cycle time
- Technology Challenge  
45nm Design rules, physical verification, SI
- Design Complexity  
Functional Verification, Late RTL changes

# Late RTL change – What is the problem?

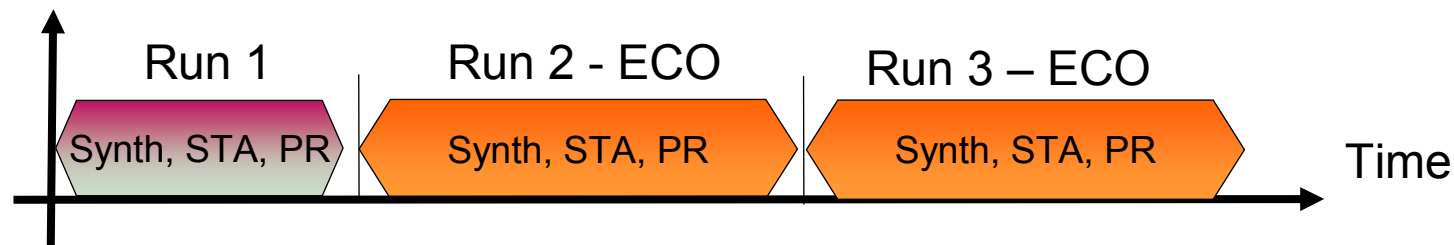


Redo this for every RTL change???

# ECO Challenges for SAPR Flow

## Challenge 1: Turnaround Time

- functional RTL change requires a complete flow re-run



## Challenge 2: Unpredictability = **RISK**

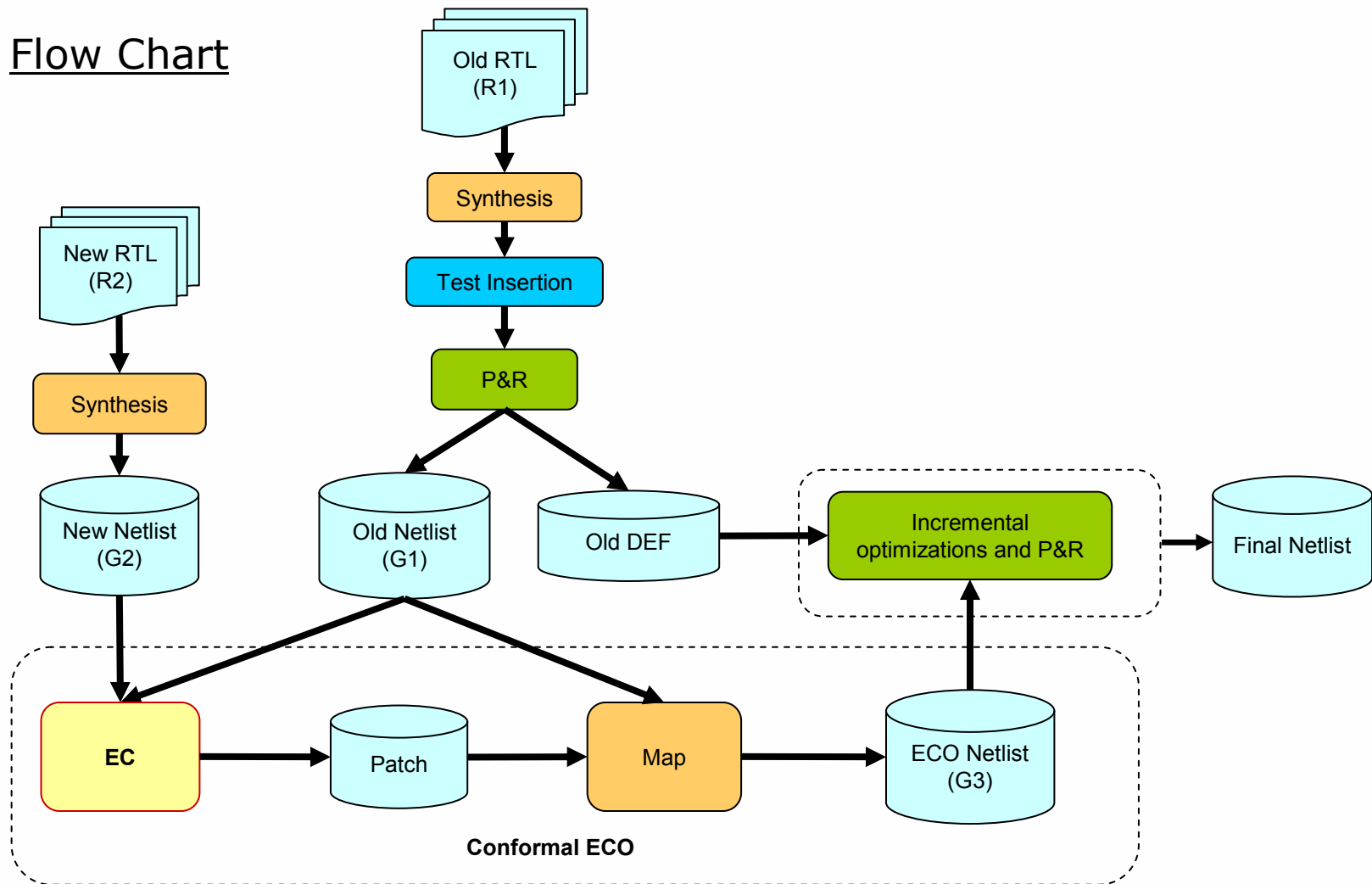
- Current ECO approach offers very little predictability  
(**like: new critical paths**)

## Challenge 3: Re-fitting with other hierarchical blocks

- Potential IF timing problems

# Conformal ECO as a Solution – How it Works

## Flow Chart

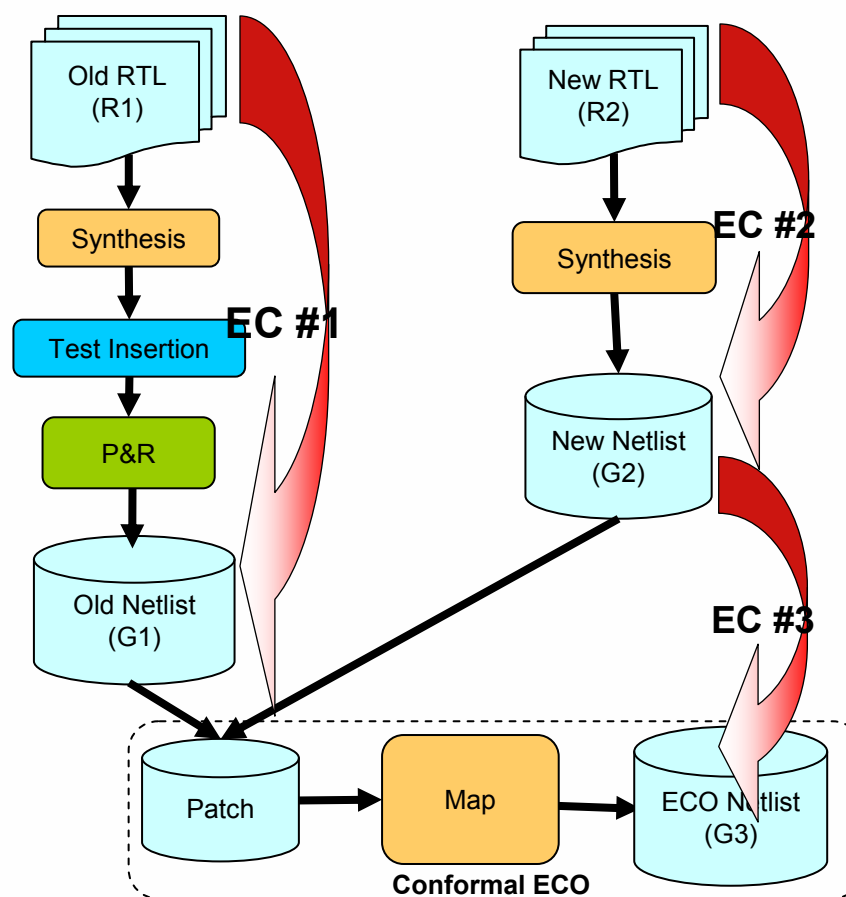




## Concern: How do I formally verify my ECO?

**Answer:** Part of the Conformal ECO flow is to run LEC to confirm 100% matching results :

1. R1 vs. G1
2. R2 vs. G2
3. G2 vs. G3



# Baseline Conformal ECO script

## # 1. step – normal LEC compare old RTL gate netlist vs new RTL gate netlist

```
<normal LEC setup/run old vs new netlists>
```

```
compare
```

```
analyze_eco <patch.file> -replace
```

## # 2. step - map the patch eco netlist

```
read_design $GOLDEN_NETL $NETL_DIR/$PATCH_NETL -verilog -sensitive -replace
```

```
add_eco_library stdcell
```

```
map_eco_patch <maped.file> -replace -noconstraint -instancenaming "ECO_%d" -netnaming  
"ECOnet_%d,,
```

## # 3. step - write out merged eco netlist

```
read_design $GOLDEN_NETL -root $MODULE_NAME -verilog -golden -sensitive -replace
```

```
read_design $NETL_DIR/$MAPED_NETL -append
```

```
apply_patch $MODULE_NAME "file_eco" -golden -report ECO.report
```

```
write_design $ECO_NETL -replace
```

## # 4. step - final compare for eco netlist vs new RTL gate netlist

```
<normal LEC setup/run new netlist vs ECO netlist>
```

# Conformal ECO Evaluation Results



<b><u>Design</u></b>	<b><u>Size</u></b>	<b><u>ECO @ RTL</u></b>	<b><u>Conformal Patch Size</u></b>	<b><u>Run Time</u></b>
Block A	37K instances	Insert 4 DFF(s) and modify 4 "assign" statement	// 12 library cell(s) are in the patch  // 4 DFF(s) are in the patch	442 sec
Block B	2.2 K instances	Insert 64 inverters into a 64-bit select line	// 1 library cell(s) is freed	25 sec
Block C	752K instances	Replace a "  " with "&&"	// 3 library cell(s) in the patch	6 sec
Block D	67K instances	Insert an inverter into an "assign" statement	// 4 library cell(s) in the patch	100 sec

# Conformal ECO Put-to-the-Test (& Results)



## Enhancement requests during the evaluation

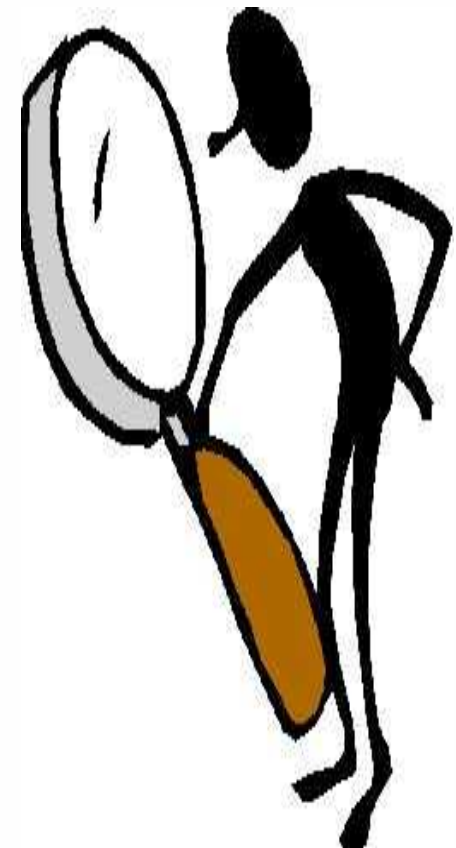
- Ease-of-Use:
  1. add a prefix string to ECO'ed instance and net names. **IMPLEMENTED**
  2. detail report of new/recycled/freed cells. **IMPLEMENTED**
  3. provide a list of *dont-use* cells, in addition to understand the *dont-use* attribute in liberty library **IMPLEMENTED**
  4. create new ECO primary inputs and outputs, or convert single port to bussed port and vice versa **IMPLEMENTED**
  5. Re-arrange the ECO netlist (G3) format, easily view the delta among G1 vs G3 netlists **Plan Release: 7.2**
- Quality of Result:
  1. Improve the patch size [i.e. # of ECO gates needed] for same or comparable to a manual ECO. **IMPLEMENTED**

# Results from our ECO flow

	Design A	Design B
Design data	Leaf Cell # 82,400 Final Utilization 67% Final DRCs 0	Leaf Cell # 185,100 Final Utilization 56% Final DRCs 0
Implementation CPU Time	Total: 55 min  (Psyn 200s, Place 410s, CTS/Hold 1150s, Route 1590s)	Total: 490 min  (Psyn 3921s, Place 8430s, CTS/Hold 8690s, Route 8406s)
RTL change/Patch size	Add FSM state  (56 leaf cells)	increase FSM counter size  (67 leaf cells)
ECO implementation time	Total: 22 min  LEC: 13 min  Physical ECO: 9 min	Total: 157 min  LEC: 52 min  Physical ECO: 105 min

## Summary

- SAPR flow requires by each RTL change a complete re-run of the flow
- Causes unnecessary challenges and long turnaround time
- An **incremental approach** is an extension to the existing SAPR flow to handle ECOs
- A more **automated** solution using Conformal ECO has been successful



## Benefits

- ✓ Incr-SAPR flow is now in BETA with Conformal ECO integrated
- ✓ as the solution to handle ECOs without performing a complete re-run of SAPR each time

↓ **RISK**

↑ **Predictability**

- ✓ This process is **repeatable** and is **time saving**, ability to reduce ECOs to less than a day

# Q & A

*Thanks for your attention!*

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