common platform™

IBM Chartered SAMSUNG

Cadence 65nm Low-Power Reference Flow for Common Platform Technology

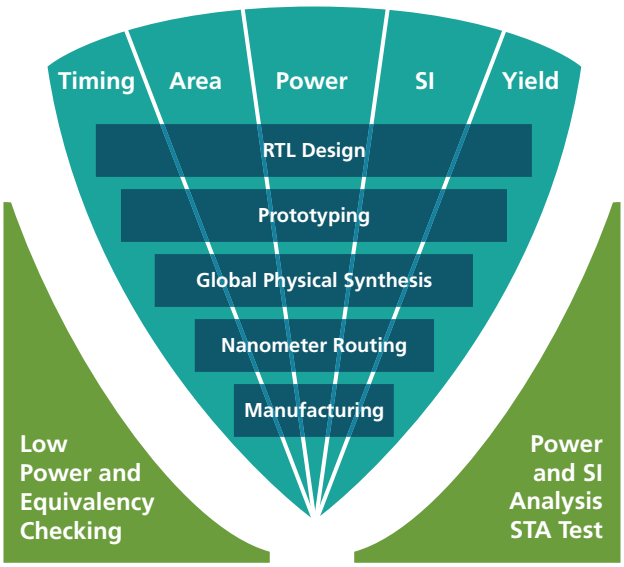
Overview

As the industry moves to 65 nanometers and below, the challenges related to the design and manufacture of low-power products have increased exponentially. In response to these challenges, the Common Platform™ technology collaborators and Cadence Design Systems have developed a 65nm low-power reference flow using the Si2 Common Power Format (CPF) standard to provide a single specification of low-power intent throughout the flow.

Developed as a logical response to the unique and escalating demands of the 65nm process, the RTL-to-GDSII flow was developed through close collaboration among IBM, Chartered Semiconductor Manufacturing, Samsung, and Cadence Design Systems.

This reference flow delivers a comprehensive methodology for addressing complex design issues such as exponential increases in leakage power and the need for advanced power optimization strategies, as well as new design for manufacturability (DFM) challenges.

Based on the ARM® Metro™ low-power products—part of the Artisan® family of Physical IP—the Cadence 65nm Low-Power Reference Flow was created to facilitate high-yield, high-volume production of advanced low-power designs. An Encounter-based solution, the flow addresses nanometer defect and yield issues with a proven suite of analysis and optimization capabilities embedded at critical implementation stages, including concurrent routing and dual via insertion, leakage power-reduction strategies, and process-variation extraction issues.



CPF-Enabled Encounter Digital IC Design Platform

Common Platform Alliance

The unique collaboration among IBM, Chartered Semiconductor Manufacturing and Samsung Electronics makes possible worldwide multi-sourcing of a single design at any of the companies' synchronized 300mm manufacturing facilities.

Because of the broad-ranging manufacturing and systems expertise of each company, Common Platform collaborators can help resolve complex technical and economic challenges in chip design and manufacturing. The benefits include GDSII compatibility, advances in low-power design, time-to-market efficiencies, and high-volume manufacturing.

The leading-edge, bulk CMOS process technologies (standard and lower-power) in 90, 65, 45 and 32 nanometers are supported by a comprehensive ecosystem, which includes design enablement and implementation partners from EDA, IP, packaging and design services companies.

Designers now have both choice and flexibility with this open industry foundry model.

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Meeting industry challenges at 65nm and below

As time-to-market cycles continue to shrink, the need for advanced design tools has become critical. Increased time pressure, the need for power-efficient designs and the threat of cost overruns have sharpened the need to uncover and correct potential problems early in the physical design cycle. Design revisions or production delays can cause millions of dollars in cost overruns, underscoring the need for design and manufacturing to correlate as closely as possible.

As demonstrated in the reference flow, Cadence supplies a comprehensive family of EDA tools designed to meet these challenges. At each stage of the process, from design floorplanning to tapeout to chip finishing, key Cadence technologies are there to assist design teams in developing low-power designs for today's demanding requirements.

Key Cadence technologies used in implementing the Cadence 65nm Low-Power Reference Flow for the Common Platform technology include: Encounter Conformal® Low Power, RTL Compiler, SoC Encounter™ RTL-to-GDSII system, Encounter Timing System XL, NanoRoute Ultra nanometer router, VoltageStorm® power analysis, and Cadence QRC Extraction.

Features and benefits

- Multifaceted collaborative strategies for advanced low-power design solutions across the Common Platform technologies ecosystem
- Scalable and holistic methodology using CPF enables multiple power optimization techniques to increase design team efficiency and productivity
- Voltage domain-aware technologies supporting power shut-off
- Multiple mode/multiple corner (MM/MC) timing closure, automatic decoupling capacitor insertion, and dynamic IR drop analysis
- Leakage and dynamic power optimization based on ARM Metro 10LP Multi-Vt libraries
- Encounter Timing System to achieve timing convergence across the flow
- Design for Test (DFT) techniques provide measures to comprehensively test the manufactured device for quality and coverage. Key DFT techniques used in this reference flow include Scan insertion and stitching
- DFM solution supports yield-enhancing techniques such as wire spreading, double-cut (dual) via optimization, DRC rule routing, half-track wire spreading, and critical area analysis

cadence™

Cadence enables global electronic-design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software and hardware, methodologies and services to design and verify advanced semiconductors and system design. To address the emerging importance of low-power designs, Cadence has launched industry's first complete flow that integrates logic design, verification, and implementation technologies for the low-power SoCs. By using Cadence Low-Power Solution in conjunction with Si2-approved Common Power Format (CPF), design teams can improve productivity, reduce risk, and achieve superior tradeoff among timing, power, and area requirements.

Cadence reported 2006 revenues of approximately $1.5 billion and has about 5,200 employees. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at www.cadence.com.

To learn more

Find out more about the Cadence 65nm reference flow, please send an email to **common_platform_65LP@cadence.com**