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Interview: Low-Power Design and Verification using CPF

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An Interview conducted by Stylianos Diamantidis, Verification Zone Moderator, CDNusers.org
Low power design is undoubtedly a major concern for virtually any design project. As chips get more complex, low power design verification has emerged as a key challenge to first-silicon success. In this interview, Stylianos Diamantidis, CDNusers.org forum moderator, talks to Milind Padhye, Wireless Low Power Design Manager at Freescale Semiconductor and Power Forward Initiative (PFI) advisor. Milind describes some of the challenges of designing and verifying low-power ICs, as well as how the Common Power Format (CPF) industry standard can be used to drive the verification process.

Stylianos: What is Common Power Format (CPF) and what is your role as Power Forward advisor?
Milind: CPF is the lifeline of Low Power Design. CPF is a consolidated description of low power intent throughout the entire design flow. It drives a consistent integration and verification of all low power features in the design. As a PFI advisor, I work closely with all members to ensure that low power design needs are properly addressed.

Stylianos: What are some of the challenges of designing low-power ICs?
Milind: Conventional flows reached a bottleneck with advanced low power techniques. Verilog could not capture the power net connectivity to establish a fully consistent flow for integration and verification. Verifying low power features at RTL has been a significant bottleneck. Design productivity can be significantly impacted if the power related issues are found at a very late stage.

Formal verification of low power features has been another challenge. Special tools and flows are needed to formally verify the low power designs. Voltage variations have a significant impact to timings. Thus a multi-voltage design has created a large number of corners and analysis points. Timing convergence across multiple corners is equally challenging and can cause multiple iterations.

Debugging the low power design is a big challenge in itself. If a part of the design is powered off due to a bug, it can not be debugged any further. That part of silicon is dead. Careful analysis and debug structures are very essential for low power silicon success.

Stylianos: People consider power to be a design back-end concern. How does power design relate to functional simulation?
Milind: It would be a mistake to associate power with just back end. As I described earlier, the majority of the power saving can be achieved at a higher level of design and hence the low power intent must be verified at higher level of abstraction. It is extremely important that all low power intents are well justified and verified at a higher level.

Stylianos: How does CPF help address verification of power intent?
Milind: CPF describes the intent. The power shutoff and wakeup conditions are identified by a simulator accordingly to update the state of various nodes and state machines in the design.

A dedicated Global Power Controller module is responsible for managing power-up and power-down sequences inside the chip. It is a major part of the Power Control Diamond. The GPC interacts with various cores, IPs, clock controllers and mentors the power state of the chip. Verification testbenches use the GPC in conjunction with CPF to drive all signal sequences and verify the power intent at standalone and chip level.

Stylianos: How about design IP? How does CPF work when integrating soft or hard IP?
Milind: CPF enables both soft and hard IP integration. The IP provider represents the power intent of the IP in CPF. All module level CPFs are sourced at chip level and appropriate design infrastructure is created to support the IP low power needs. A Power Controller Module is integrated at the chip

level to provide appropriate sequences and modes for low power operations of all IPs. New hierarchical flow capabilities with CPF are under consideration.

Stylianos: What direct benefits has your design group seen from using CPF?
Milind: I have quoted this earlier too! One bug related to power intent could be almost equivalent to fixing 10 functional bugs. When debugging power on validation boards, it is not simple. Not every power node is observable and hence debugging is a complex issue with limited observability of power. If such mistakes can be avoided by simulating at early pre-silicon design phase, it is major savings to design turn-around costs and overall product ramp-up time.

CPF enables a consistent low power design integration and verification flow. This reduces expensive errors and improves the low power concept to silicon cycle time.

About the author

Milind Padhye is Low Power Design Manager at Freescale Semiconductor, Wireless design organization. He has been working in the field of low power design for last six years and has multiple patents on power reduction techniques and integration. He has lead multiple chips for low power architecture and design. Milind holds MS-EE from IIT Kharagpur, India in 1990.

Stylianos Diamantidis is a founder of Globetech Solutions, a premier provider of design verification and silicon test IP based solutions, where he serves as Managing Director and CTO. With over 10 years of experience in design verification, he is responsible for driving IP product strategy, engineering and consulting services. Prior to Globetech, Stylianos managed system-level diagnostic software development at Silicon Graphics Inc. He has held engineering positions in design verification, test and diagnosis. Stylianos holds a B.Eng in Computer Systems Engineering from the University of Kent at Canterbury, UK, and an MS in Electrical Engineering from Stanford University.