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Session 4.1: A new Methodology to Detect Small Delay Defects in 65-nm Devices

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Cadence Design Systems

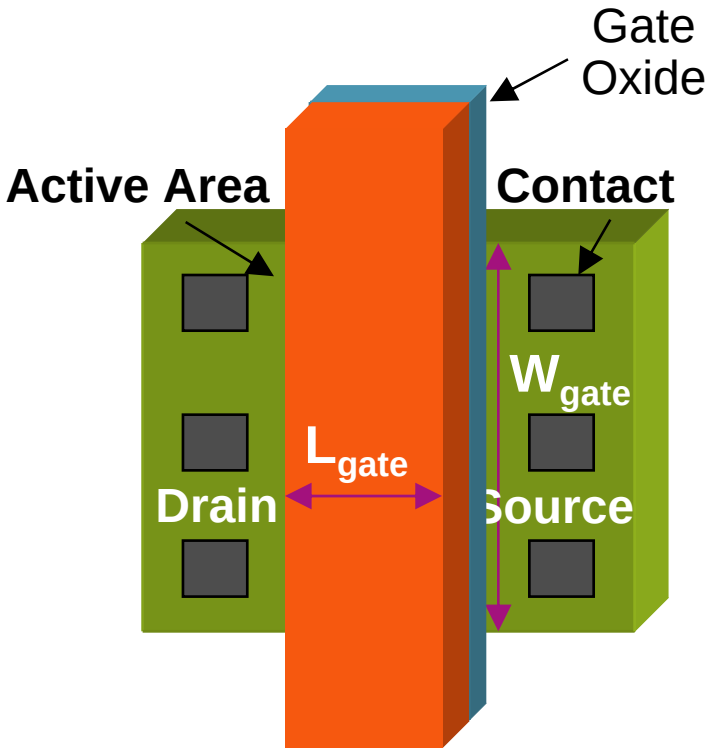
Agenda

- 65-nm challenges
  - Defects
  - Current detection methods
- Timing-Aware ATPG
  - Overview
  - Prerequisites
- Published results of applications using timing-aware ATPG
- Implementation methodology example:
  - Low Power Design
- Summary

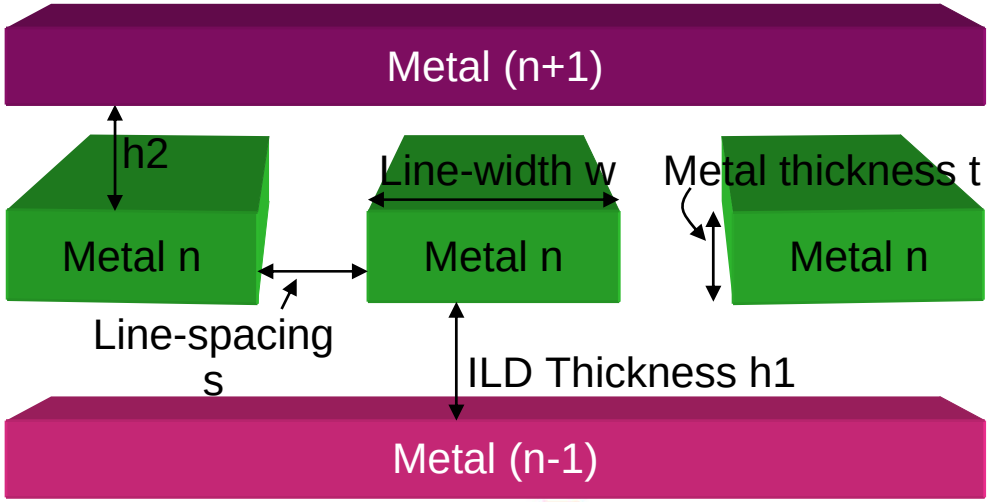
Sources of Variation

Cause Delay Defects

- **Device parameters:**
  - L_{gate} – channel length
  - V_T – threshold voltage
  - T_{ox} – oxide thickness
  - W_{gate} – Channel Width



- **Interconnect Parameters**
  - Metal thickness – t
  - Dielectric thickness – h_1, h_2
  - Metal line width (or line spacing) – w or s

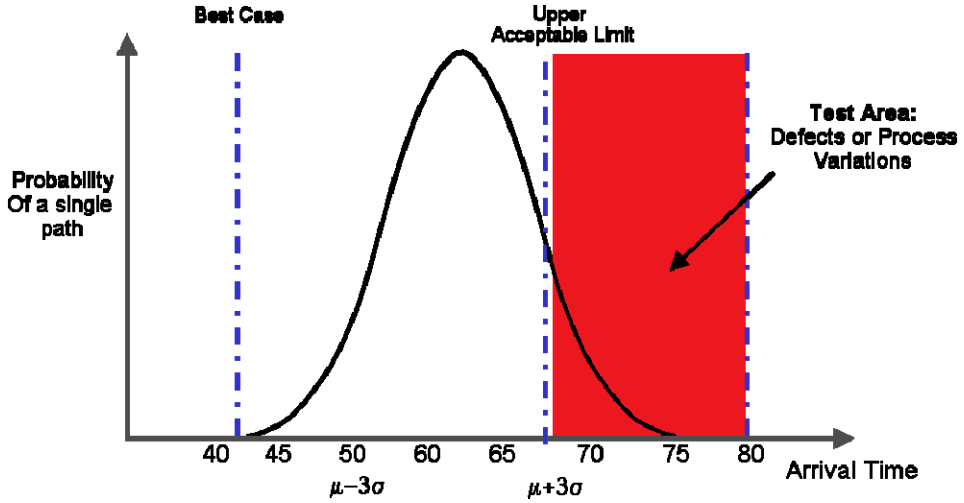


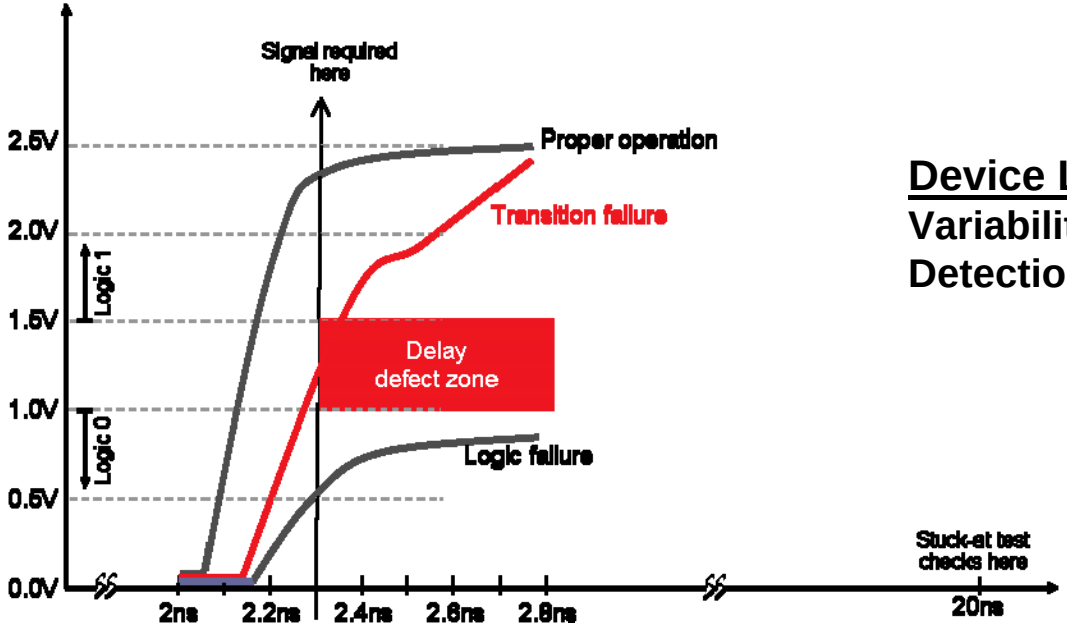
Current Detection Methods Often Fall Short
Complex Defects are Common at 65-nm

- Inline inspection & measurements
  - Signal-to-noise ratio capabilities of inspection equipment are being challenged
  - CD measurements – where to look?
  - Finding real defects among a large number of false defects is difficult
- Parametric testing
  - Delineating actual defects from parametric process variation is expensive and sometime prohibitive
- Standard electrical testing
  - Stuck-at fault models cannot readily detect delay defects
  - iDDQ testing is less effective due to high leakage currents
  - Functional testing is expensive and non-deterministic
  - Fixed cycle transition testing can miss small defects
  - ATPG cannot always excite the longest path

Impact of Variations
Require the Use of Timing-Aware ATPG

Wafer Level (die to die path timing)
Variability: Individual path slack timing varies
Detection: Dependent on which path is tested





Device Level
Variability: Slow rise/fall of individual signals
Detection: Dependent on capture time

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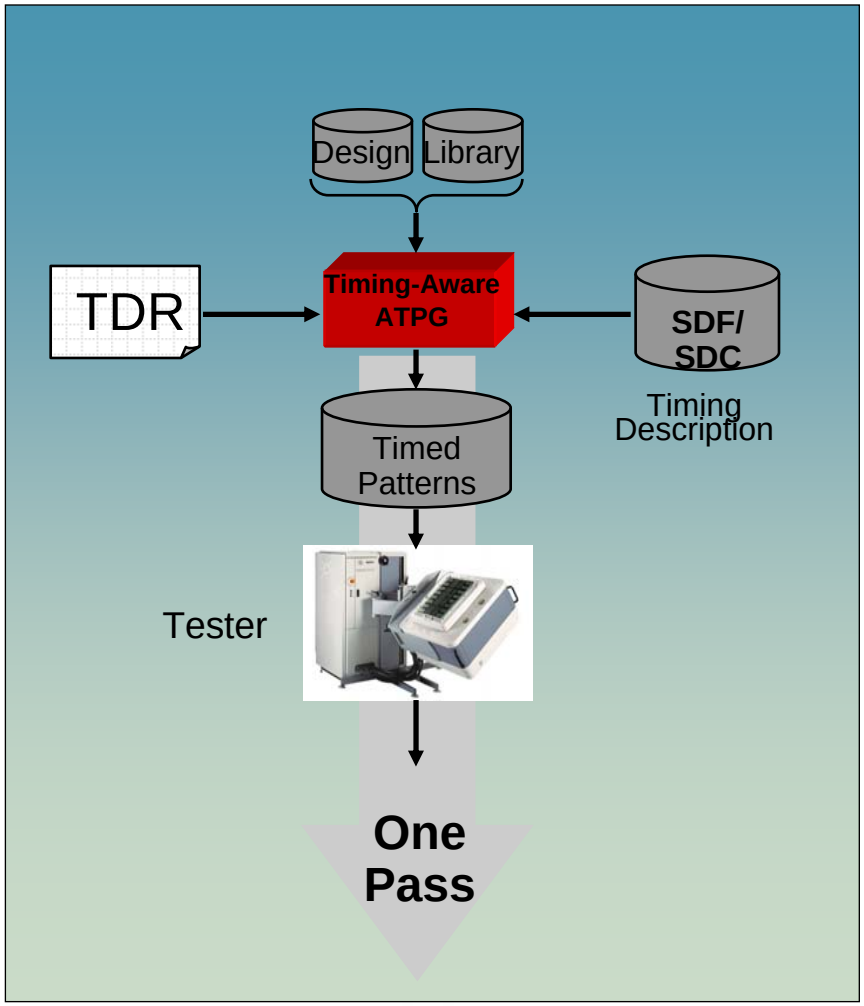
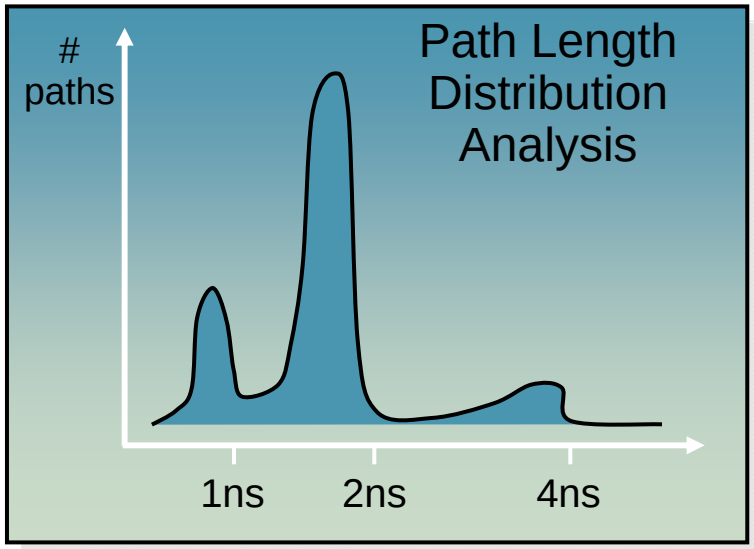
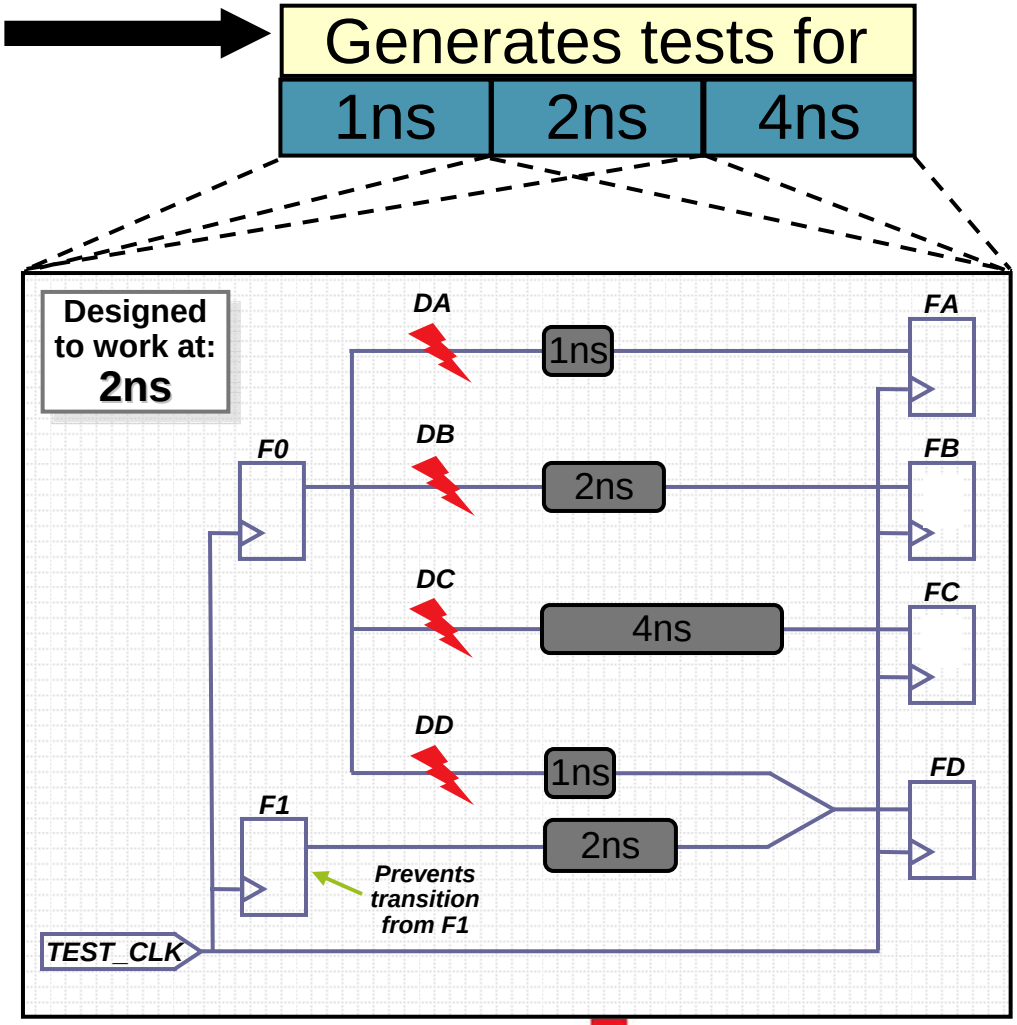
Supplementary Timing Data

- Standard Delay Format (SDF)
  - Is a standard output from almost all static timing tools
  - SDC defines constraints
  - Includes best, nominal, and worst case timings, as well as setup and hold timing checks
  - Generated for test voltage, temp and other conditions
- Tester Description Rule (TDR)
  - Number of clocks and timing sequences
  - Frequency limits, phase and frequency accuracy
  - Edge placement accuracy for switching signals and pulsing clocks



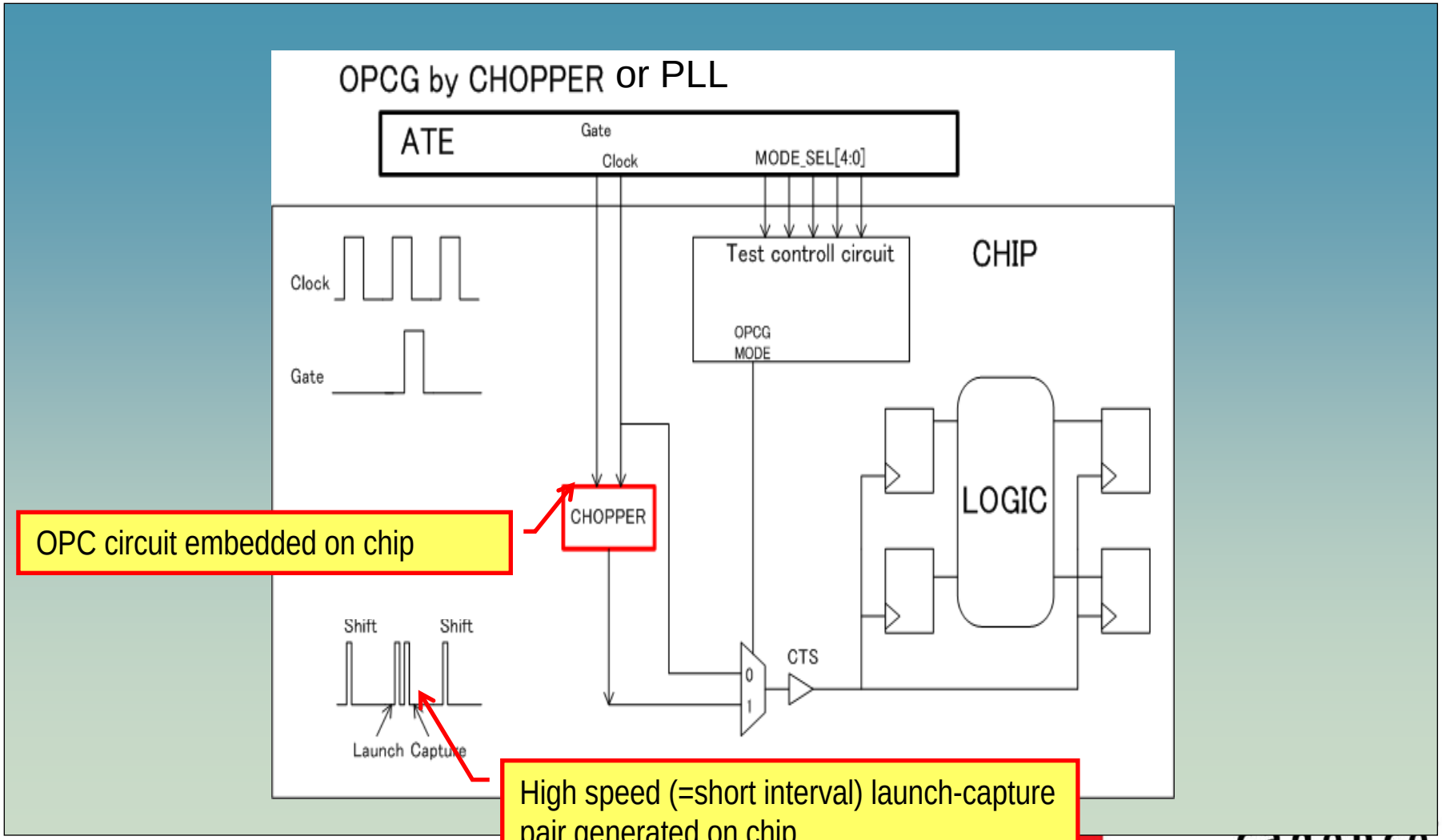
Timing-Aware ATPG: Test for Delay Defects





- Actual delay timings (clock distribution, IO pads) used to determine domain timings
- Separate test can be generated for each domain timing
- Test for shortest domain generated first
- FF's capture long path marked capturing X
- Long and short paths to same flop can be tested independently (to improve coverage)

On-Product Clock Generation – OPC
Required for Faster Than At-Speed Testing



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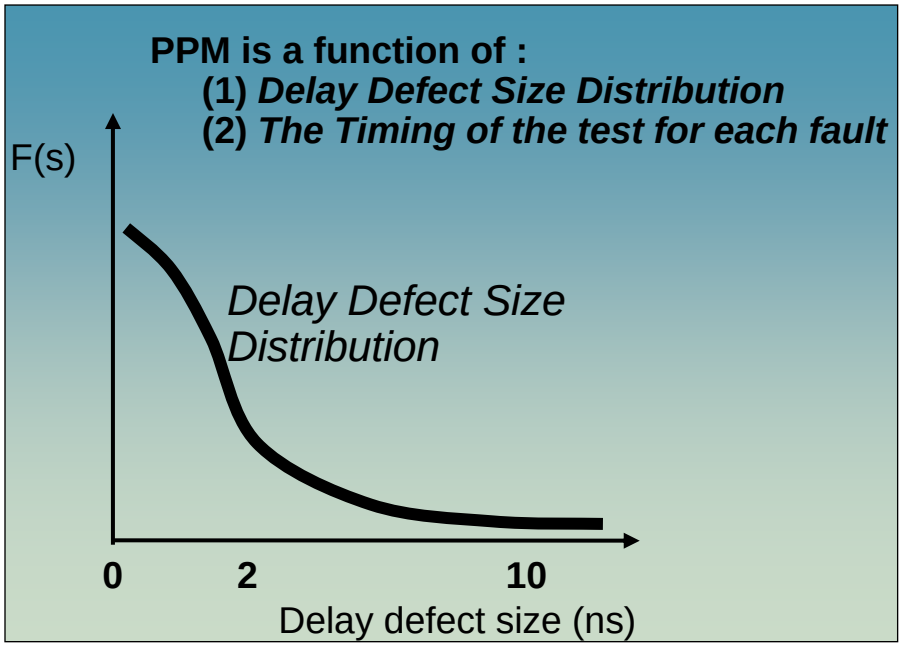
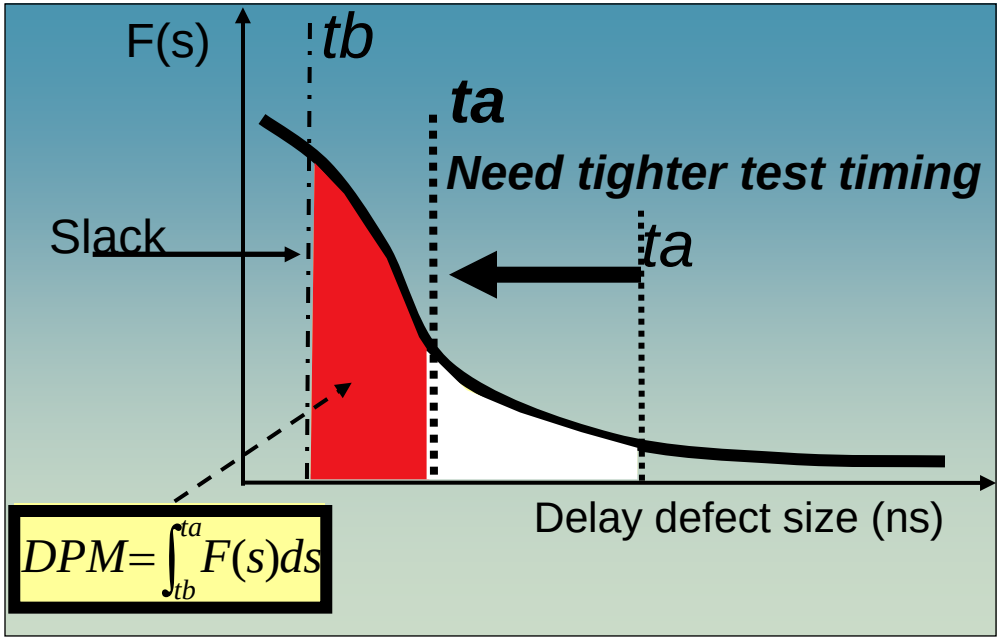
PPM Prediction Model for Delay Test
Statistical Delay Quality Model

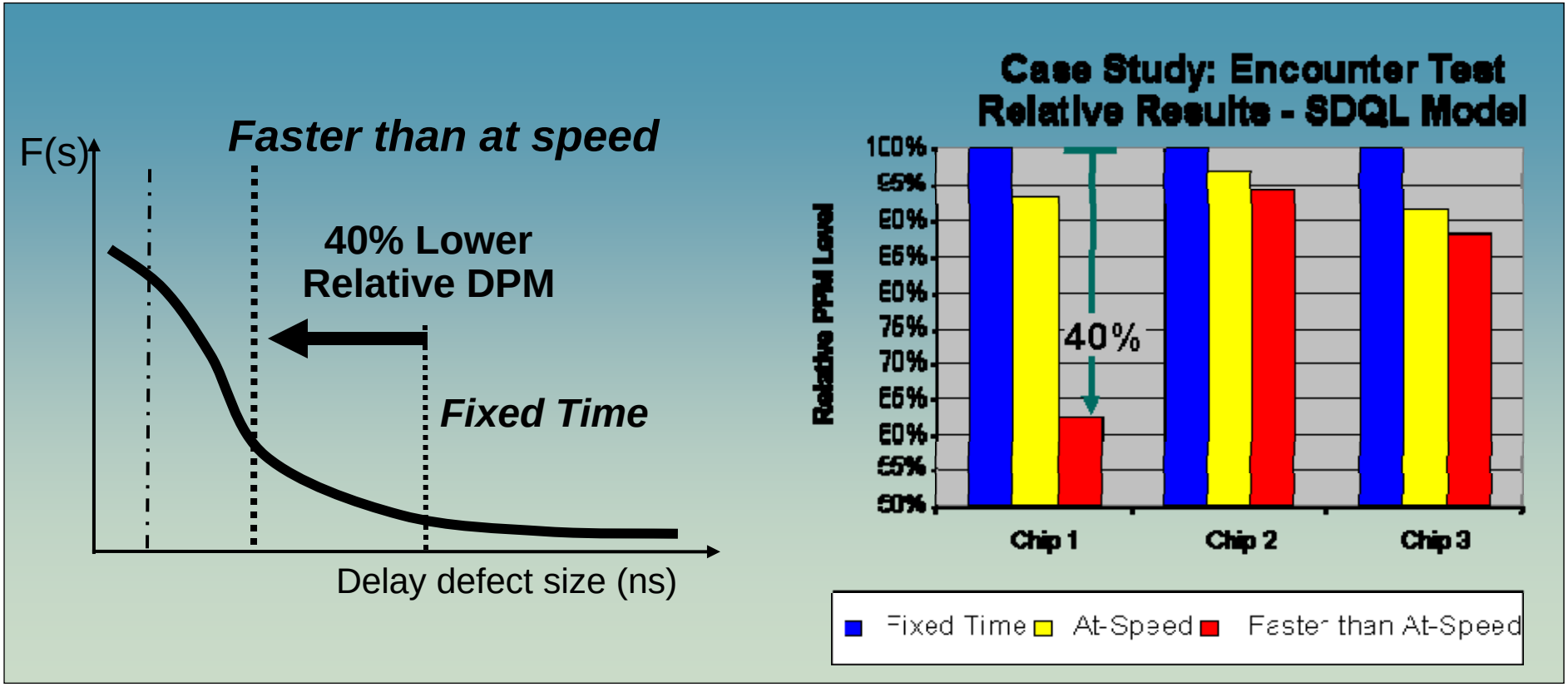
- Objective: quantify the effectiveness of a given delay test method
  - Defects Per Million (DPM) is a measure of test escapes (aka SDQL, PPM, Defect Level)
  - Test A %cov = Test B %Cov *BUT* Test A *DPM* < Test B *DPM*
  - Model is from STARC - consortium co-founded by eleven major Japanese semiconductor companies





Model Source: STARC - a consortium co-founded by eleven major Japanese semiconductor companies; Sato et al, ASP-DAC05

Example
Quality Level with Faster Than At-Speed Testing
Case Study Results with STARC Model



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Example
Finding Test Escapes with Faster than At-Speed

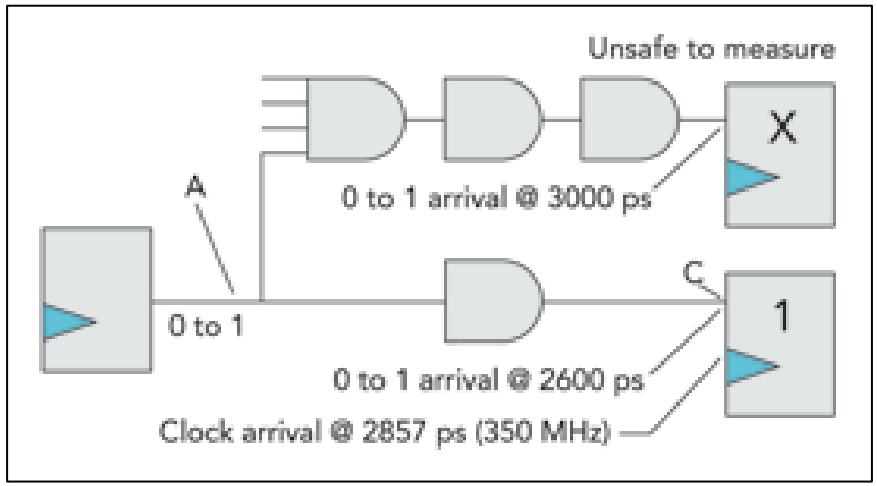

Figure 2. Faster-than-at-speed testing removes slack along the path from A to C and permits detection of a fault at A. For this testing to succeed, however, flip-flops on longer paths must be masked.

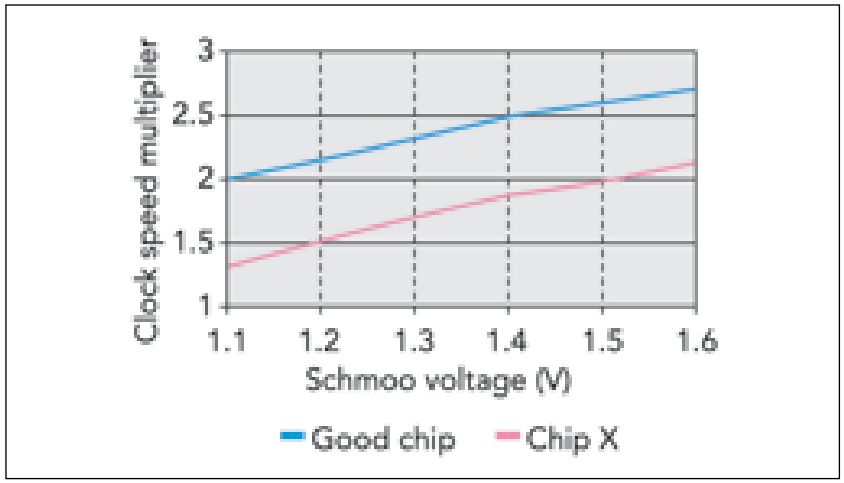

Figure 4. A delay defect on chip X caused it to begin exhibiting failures at 1.7X the clock frequency at its 1.33-V nominal operating voltage. A good chip tolerated a 2X clock even at 1.1 V.

Source: Beyond at-speed Martin Amodeo, Cadence Design Systems, and Bruce Cory, nVidia -- Test & Measurement World, 11/1/2005

Testing the Chip by Domains Improves Quality

Circuit A (Logic Size 3.3Mgate, Max Freq. 300MHz)		
Clock Domain (Frequency)	Pattern length (MBytes)	
	Domain by domain ATPG	ATPG for entire chip
CLK1 (300MHz)	1.20 (FC: 13.89%)	18.90 (FC: 88.86%)
CLK2 (150MHz)	1.10 (Accumulated FC: 65.19%)	
Others	12.00 (Accumulated FC: 88.86%)	
Total	14.30 (Overall FC: 88.86%)	

Low Cost Delay Testing of Nanometer SoCs Using On-Chip Clocking and Test Compression

ITC 2004: Hiroyuki Nakamura Akio Shirokane Yoshihito Nishizaki Kawasaki Micor; Brion Keler, Anis Uzzaman et al Cadence Design

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New DFT Methods are Required for 65-nm
Low Power adds additional complexity

- Reduction in iteration times across design verification, power, test, physical
  - Early DFT insertion and verification reducing tail-end loops
  - Power considerations (manufacturing test) moved to early design phase
  - Physical considerations for scan chain optimization and re-ordering after PD
  - XOR or MISR compression to reduce pattern count
- Reduction in overall front-end schedule
  - Continuous rule RTL checking and strong links to verification
- ATE consideration during test generation
  - Use ATE specs to generate tests that run on ATE

Design with Test Instead of Design For Test

- Metrics Driven
  - Coverage or PPM, cost, scan memory depth, ATE pin accuracy, power intent…..
- Synthesis with DFT
  - Single pass for scan, compression 1149.1 Memory BIST…
- Compression
  - Multi-architecture (XOR or MISR)
- Timing Aware ATPG
  - Uses actual slack times and ATE constraints
- For Low Power
  - Automatic Insertion of Low power DFT and test modes
  - Resource sharing: memory BIST
  - Power aware ATPG to limit switching

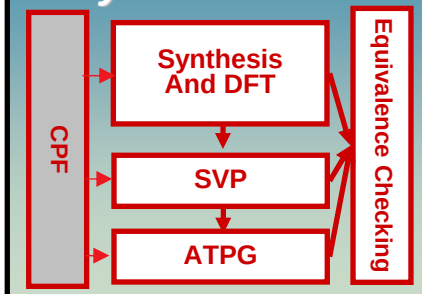
Design with Test Example

Power-Aware DFT, Test Generation, Diagnostics and Signoff

- Single pass scan flow
- Advanced DFT in synthesis flow
- Synthesis of power control structures using CPF

- ATPG validation and sign-off
- Power control verification
- Equivalence checking of pre-post DFT

Power-Aware Synthesis Flow

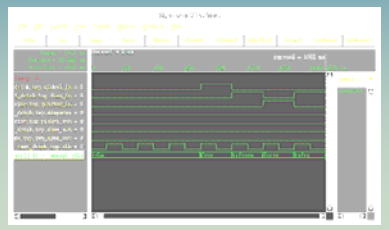


Power-Aware ATPG

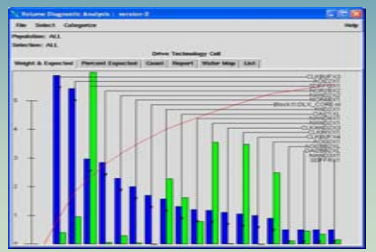
Mode	Clock (MHz)	% Switch	Power (mW)
Normal	500	10~20	2.96
Scan	50	46	11.86
LP Scan	50	6	1.66

- Encounter Test Model has test modes that reflects power modes
- Power domains verified for isolation and scan integrity
- Reduced power during test

Power-Aware Verification and Signoff Flow



Power-Aware Yield Diagnostics



- Volume mode to identify yield limiters per power domain
- Precision mode to locate root cause of defects
- Model complex defects using Pattern Fault Model

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Summary

- 65-nm test challenges are different
  - Small delay defects are common
  - Current methods do not adequate address defects
- Timing driven ATPG is required
  - Use actual circuit timing for accuracy and efficiency
  - Bin paths and test each at optimal frequency
- Design with Test
  - Metrics driven, RTL rule checking
  - Single pass DFT insertion (Scan compression, 1500, memory BIST…)
  - Power aware flow
- Higher quality and predictability

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