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Technical University of Braunschweig and Cadence

"With Cadence Academic Network, TUBS students get the education they need to succeed and we can conduct research that furthers power optimization in system design."

Mladen Berekovic, Professor for VLSI Design, Technical University of Braunschweig (TUBS)

The Cadence Academic Network Member

Technical University of Braunschweig (TUBS) is a public research university located in Braunschweig, a city in northern Germany. Established in 1558, TUBS is one of the nine leading Technical Universities (TU9) in Germany.

TUBS is a member of the Cadence® Academic Network, which was launched in 2007 to promote leading-edge technologies and methodologies at universities known for their engineering and design excellence. Network members—comprising university instructors, research institutes, and Cadence technology experts—meet to exchange expertise in the areas of verification, design, and implementation of microelectronic systems.

"The Cadence Academic Network provides members with an exciting opportunity to discuss analog, mixed-signal, and digital design and test with others in the same academic field," says Mladen Berekovic, Professor for VLSI Design at TUBS. In the Academic Network, he leads discussions and projects involving low-power digital design.

"Academic Network members meet several times per year to give presentations and launch conversations and collaborations about tools and methodologies that can be used in our current and future teaching," Dr. Berekovic says.

The Challenge

As a professor, Dr. Berekovic specializes in very-large-scale integration (VLSI)—the process of creating integrated circuits (ICs) by combining thousands of transistors into a single chip. Since the 1970s, VLSI has advanced dramatically. Today's micro-processors, for example, feature millions of gates and billions of individual transistors.

Challenges

- Prepare students for workforce by teaching with powerful electronic design automation (EDA) technologies
- Cultivate relationships with educators and corporations to further academic research in low-power digital design

Cadence Solutions

- Cadence Academic Network
- Incisive Unified Simulator
- Encounter RTL Compiler
- Encounter Digital Implementation System
- 3D Design Viewer
- C-to-Silicon Compiler

Results

- Students earn internships and jobs at leading technology companies with a strong presence in Europe
- TUBS participates in publicly funded research projects involving low-power digital design

To teach his students, Dr. Berekovic needs access to the most powerful electronic design automation (EDA) technologies available to the market. He must help his students to master industry-standard solutions they will encounter during internships and in the workforce.

In addition, Dr. Berekovic must pursue and cultivate relationships with other educators and corporate representatives to further academic research efforts that aid not only his students, but also the industry at large.

The Solution

Dr. Berekovic has several interactions with Cadence in both academic and research settings. First, he uses Cadence technologies and platforms to teach practical, hands-on chip and system design in the classroom. Second, he participates with Cadence in publicly funded research projects.

Teaching

VLSI lectures taught by Dr. Berekovic range from the theoretical background of VLSI and an introduction to digital IC design to the concepts of system design. Labs provide opportunities to apply practical knowledge of modern standard-cell synthesis flows and electronic system-level design.

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In the introductory lab, Dr. Berekovic uses Encounter® RTL Compiler, Incisive® Unified Simulator, and Encounter Digital Implementation System to teach an understanding of modern standard-cell synthesis flows. Using these Cadence solutions, students implement a micro-controller in VHDL, develop testbenches, and synthesize the design down to place-and-route.

"Encounter Digital Implementation System offers complete and integrated digital design, implementation, and verification for developing large-scale, complex systems-on-chip (SoCs)," Dr. Berekovic says. "This Cadence solution enables me to teach my students how to produce advanced low-power and mixed-signal SoCs at leading-edge process nodes."

In an advanced lab, TUBS students develop a JPEG compressor in the form of a virtual platform using Cadence solutions. "Students develop a system that contains an ARM® 9 subsystem, an Open Core Protocol (OCP) system bus, multiple input/output peripherals, and a dedicated DCT accelerator," Dr. Berekovic says. "During this lab I rely heavily on Incisive Unified Simulator for register-transfer level (RTL) and SystemC™ co-simulation."

Becoming proficient with Cadence solutions helps TUBS students land sought-after internships and jobs at technology companies with a strong European presence.

Research

Dr. Berekovic's relationship with Cadence through the Academic Network enables him to participate in publicly funded research projects in his area of interest—low-power digital design. "If we have a concept for a circuit, a company will often pay for us to investigate the idea," he explains. "Currently, TUBS is involved in research projects for Infineon and ST Microelectronics."They have has also been collaborating with Silicon Hive on low-power methodologies.

Cadence 3D Design Viewer provides opportunities for TUBS to participate in high-level research work. "If a company wants to see a realistic visualization of how a design will look in silicon, we can use 3D Design Viewer to quickly see the results," he says. Engineers can pan and zoom in on an image from any angle, explore the design in detail, take snapshots of the screen, and use built-in annotation tools to add shapes, arrows, and text.

Dr. Berekovic also frequently uses Cadence C-to-Silicon Compiler, a high-level synthesis product that supports the creation and reuse of SoC intellectual property (IP). This product helps bridge the gap between RTL models—commonly used to verify, implement, and integrate SoCs—and system-level models, usually written in C/C++ and SystemC languages.

The TUBS research group is also working on system-level design methodologies for future multi- and many-core on-chip systems. In a project with SiliconHive and ST Microelectronics the group is investigating how to do automated synthesis at the system level, where performance, area, and power are considered.

Summary

Dr. Berekovic's involvement in the Academic Network enables him to interact and share knowledge with representatives from Cadence and other leading universities. He also gains access to powerful, industry-leading EDA methodologies to further TUBS teaching and research.

"I wouldn't be able to do any research if I had to use free tools," Dr. Berekovic says. "With the Cadence Academic Network, TUBS students get the education they need to succeed and we can conduct research that furthers power optimization in system design."