cadence®

Renesas and Cadence

"Our goal was to minimize area while meeting latency, throughput, and frequency goals. Despite the design's mixture of control and datapath, we were able to explore latency-area tradeoffs using C-to-Silicon Compiler and determine the optimal architecture within just half a day."

Osamu Tada, Senior Chief Engineer of Design Technology Division, Renesas Technology Corporation

The Customer

Renesas Technology Corporation—a joint venture of Hitachi Ltd. and Mitsubishi Electric Corporation based in Tokyo—is one of the largest manufacturers of highly integrated systems on chip (SoCs).

The Renesas System-Level Design and Verification Technology Department (SLDVTD), part of the Design Technology Division of the company's Design and Development Unit, is chartered with improving quality and efficiency for integrated circuit (IC) front-end design by identifying promising new electronic design automation (EDA) technologies, and getting such technologies adopted by Renesas design groups.

The Challenge

Like most companies in the semiconductor industry, Renesas faces challenges such as accurately getting complex specifications of the application, verifying the system with software, and dealing with shorter market delivery windows. The spec-to-RTL design stage consumes the most engineering resources. These considerations motivated Renesas engineers to seek ways of starting the design process from a high level of abstraction.

A key requirement for system-level design is having a robust and reliable way to translate high-level descriptions to register-transfer level (RTL) descriptions. High-level synthesis (HLS) tools have been widely available and tested in Japan since the early

Business Challenges

- Complex specifications and software verification needs
- Short time-to-market window

Design Challenges

- Improve productivity in creation and retargeting of RTL designs
- Migrate to a new system-level design methodology based on next-generation high-level synthesis (HLS)

Cadence Solution

- C-to-Silicon Compiler
- Cadence Services

Results

- A complete TLM-to-GDSII implementation flow in a single environment
- 5x shorter turnaround with design changes and subsequent verification
- Cadence HLS technology refined for next-generation production based on feedback from Renesas engineers

2000s. But Renesas was unwilling to accept the typical limitations imposed by conventional HLS tools, which were relegating them to niche applications. Two major hurdles Renesas engineers kept coming up against were the inabilities of HLS tools to synthesize designs with complex control and to support incremental synthesis/engineering change orders (ECOs).

The Solution

Renesas had looked into HLS technologies from many different vendors during previous years, but Cadence® C-to-Silicon Compiler was the first technology Renesas found that could synthesize both control and datapath designs and also support incremental/ECO synthesis.

"We examined many HLS tools in the early days and were disappointed with the quality of results and the support for incremental synthesis," says Osamu Tada, Senior Chief Engineer of the Renesas Design Technology Division. "When we were presented with Cadence C-to-Silicon Compiler technology in early 2005, we thought this could be the solution for our requirements."

Renesas engineers estimated that if they had been working with manually created RTL, those design changes and subsequent verification activities would have taken about five times longer.

Cadence also offered a complete transaction-level modeling (TLM)-to-GDSII implementation flow under one roof. Renesas saw major potential value in applying such technology to "real" projects. And to minimize risk, the company could leverage the expertise of Cadence Services, which offered a high level of support.

"Cadence provides a comprehensive portfolio of EDA tools and services," Tada says. "We were not so interested in a point tool. Rather, we saw the potential to work with Cadence to achieve a complete system-level solution. We were very open to a long-term partnership."

Renesas tested the capabilities of C-to-Silicon Compiler with two "shadow projects," using Renesas production designs. They duplicated parts of a real production design and applied C-to-Silicon Compiler to those aspects of the design in a parallel shadow project. This would allow the project to realize substantial cost and schedule benefits, while also eliminating risk.

Starting from a paper specification, the Renesas-Cadence team created a SystemC™ model with the goal of completing the RTL for an image processor design within one month, and RTL verification a month later.

"The design was a multi-stage pipeline circuit, and our goal was to minimize area while meeting latency, throughput, and frequency goals," Tada explains. "The circuit contained a relatively simple input/output protocol, including one synchronous reset, one asynchronous reset, and a pipeline stall signal. Despite the design's mixture of control and datapath, we were able to explore latency-area tradeoffs using C-to-Silicon Compiler and determine the optimal architecture within just half a day."

The Renesas test design achieved smaller area (compared to handcrafted RTL based on a similar design), and it had shorter latency as well. Renesas engineers were also more efficient than originally expected. The number of lines in the SystemC design description turned out to be much smaller than the equivalent functionality described in RTL Verilog, and the SystemC simulation runtime was much shorter.

The Renesas team was so pleased with the results that it decided to use the C-to-Silicon Compiler-generated RTL on the real project instead of the hand-coded version. Later in the project, when it was necessary to explore other architectures to meet additional requirements, the Renesas team was able to make the necessary changes to the input SystemC source code and verify there was no adverse impact on the design—all within two days, using equivalence checking.

"If we had been working with manually created RTL, those design changes and subsequent verification activities would have taken about five times longer," Tada says.

On this design, Renesas engineers started with just algorithmic C code not initially intended for HLS. The design was a pipeline circuit similar to the first test case, with the goal of minimizing area while maximizing performance. C-to-Silicon Compiler exceeded Renesas' expectations. The team was able to rapidly synthesize a circuit that satisfied the multi-hundred MHz performance target with acceptable area.

Summary and Future Plans

With Cadence technology and support, Renesas went beyond adopting an effective high-level synthesis point tool—it implemented a comprehensive system-level design solution.

After extensive feedback from Renesas engineers, Cadence R&D and Renesas worked together to enhance C-to-Silicon Compiler for future use. They discovered ways to support simulation-based verification by identifying the manual tasks to prepare the verification wrappers for C-to-Silicon Compiler-generated RTL. They also created a verification flow with sequential logic equivalence checking (SLEC) by specifying what SLEC scripts C-to-Silicon Compiler should produce automatically.

More recently, Cadence and Renesas have collaborated to integrate TLMs with C-to-Silicon Compiler fast hardware model (FHM) generation to enable a seamless system-level design and verification flow, from algorithm to implementation. The two companies are also working together to enable power-aware micro-architecture exploration and synthesis to allow system-level tradeoffs among power consumption, cost, and performance.