cadence™

Interview: Making Reliable Models for SSTA

From cdnusers.org on 10 September 2007

Prashant Maniar, co-founder and chief strategy officer of startup Stratosphere Solutions, Inc, includes guiding the company to meet customer needs, partnership building, coffee making, network wiring, and furniture moving as part of his day-to-day job description. After talking to him, we don't doubt his energy to do it all!

cdnusers: Please tell us about your company.
Prashant: Stratosphere Solutions was founded three years ago with a vision to reduce the impact of variability on IC performance and parametric yield. To that end, we provide a toolset comprised of sophisticated variability characterization test chips and variability modeling software tools. The goal, really, is to bring a process-intelligent statistical model into the design flow.

cdnusers: What are your customers telling you about design challenges they are facing with lower node designs?
Prashant: There are a huge number of challenges at the 65 nm and below design level—both at the front end (e.g., ESL) and at the back end (e.g., DFM / DFY) where you are trying to manage the impact of smaller geometries on performance. Given that we work toward the back end, I will focus on that.

Basically, the challenges are due to fundamental laws of physics—the impact of variability is much greater at smaller geometries, requiring designers to put in a lot of guard bands and margins. Faced with challenges at lower process nodes, the question our customers are asking is: why migrate to a smaller geometry if variations cause performance to be left on the table or die size increases?

To answer that question, we have to solve variation problems. At 45 nm, the current methodology of process characterization, modeling and STA, is not a good predictor of performance in the presence of variability.

cdnusers: Why?
Prashant: STA is deterministic in nature and it is not the solution for handling the impact of variability on performance. If you look back over the last couple of years, both academia and industry representatives have cited many examples of STA use resulting in over design or lower performance or parametric yields. A lot of this has to do with the fact that in STA you assume a worst-case condition—unless you have an accurate picture of what the variations are, you have to

design to worst case.

cdnusers: So, what is the answer?
Prashant: At 45 nm and below, advanced users are looking at Statistical Static Timing Analysis. Timing analysis has historically been focused on within-die analysis, for predicting the performance of a particular part. At 45 nm, it is within-die variability that is causing the parameter distributions to be so broad. What we have to do is to start considering parameters as distributions versus mean values or individual deterministic values.

SSTA, I believe, is the fundamental mechanism for considering these input parameters as distributions. It applies statistical techniques to predict a stochastic response of the circuit under consideration while considering input parameters as random variables.

cdnusers: Please explain that.
Prashant: At a high level, let's say you have a path with a bunch of gates. Historically, you would consider each input parameter as deterministic—as a single value that is typically the mean. With SSTA, you can consider these input parameters as distributions and, then, you can apply statistical techniques to figure out the output distribution of that path in consideration.

To go a little deeper we ask: what are the things that are considered as random variables, or what does statistical static analysis mean? It means considering probabilistic distributions for devices and interconnects, considering parameter correlation such as how does Vt correlate with Ion or how does Vt vary across the die or wafer.

By using SSTA, you can increase the accuracy of the prediction of the distribution of performance. You can consider how spatial correlation, meaning how a parameter value changes spatially across the wafer, and how systematic variation versus random variation impact the parameters under consideration.

cdnusers: What other advantages are there to using SSTA versus traditional STA?
Prashant: The fundamental advantages of using SSTA are improved design margins, higher timing yields and a better prediction of the distribution or statistical performance of the circuit under consideration. That is, you are better able to predict the distribution or the performance of the circuit in the presence of the variability.

cdnusers: What products does Stratosphere Solutions provide to support the SSTA process?
Prashant: We have two products important to SSTA users—StratoPro and Ozone—that integrate to Cadence ETS and other tools. StratoPro is used by fab engineers to generate the data necessary for the modeling groups to build the models. In essence, it affords the fab a practical solution for characterizing variability. It has been designed to generate within-die statistics of electrical parameters with very, very high resolution while supporting many complex design topologies.

Now what do you do with so much data? That is where Ozone comes in. Ozone is the consumer of this rich data set—it sifts through the data to separate out sources and types of variation such as systematic versus random, die-to-die versus within-die, and then goes ahead and builds a statistical model that is suitable for feeding into tools such as SSTA. It is used by modeling groups to build a statistical model of the process.

cdnusers: Who will benefit from this solution the most?
Prashant: That is a very good question. What is happening is that the whole methodology is changing from a deterministic flow to a statistical flow. So, different components of the flow will benefit different people, but in the end it is the whole value chain in the industry that is going to benefit.

The design engineer benefits by having accurate models that support SSTA because when they tape out or sign off, they are signing off with much higher confidence. The fab benefits because they now have received a taped-out design that is signed off to a prediction much closer to what the fab is going to be able to deliver.

cdnusers: How does the Cadence/Stratosphere partnership help customers working with advanced process technologies?
Prashant: The Cadence/Stratosphere collaboration helps bridge the gap between manufacturing and design. It allows customers to develop and bring, through automated means, a process-intelligent, statistical model, into SSTA. This flow is very critical for high confidence sign-off at 65 nm and below.

cdnusers: Talk about the gap between manufacturing and design today.
Prashant: Modeling is what fills the gap between design and manufacturing. So first, you have to ask—how do mainstream model designers bring models into the statistical realm? Today, we see a lot of manual effort is going on in actually building models, but there is a lack of confidence in their accuracy. When you do this manually there is no way you can verify if the model is actually accurate.

Automation, of course, is a key benefit of the Cadence/Stratosphere partnership. If a customer is running two or three designs, the same process is being used. Creating a model automatically makes it scalable across design groups and automation around modeling helps improve the accuracy of the model. I would say there are three advantages of automating: speed of developing the models, scaling the model across different design teams, and improved accuracy.

cdnusers: How do companies deploy StratoPro and Ozone in the back-end manufacturing flow?
Prashant: If you look at the whole solution, there are three components: StratoPro for process characterization; Ozone for variability modeling; and ETS for statistical timing analysis.

StratoPro is a tool that has been used successfully by several fabs, so it is completely silicon-proven. Ozone is a new product that some of our customers are working with at the 45 nm process. We are also working with Cadence to make sure that the output of Ozone is tightly integrated into ETS.

About the author

Prashant Maniar is co-founder and chief strategy officer of Stratosphere Solutions Inc. of Sunnyvale, Calif., a startup providing yield improvement solutions to the semiconductor industry with the goal to make yield a signoff item that links design to manufacturing. Prior to founding Stratosphere Solutions, Maniar was director of marketing of the TestChip Division of HPL Technologies. Before that, he spent seven years at Synopsys in a variety of applications, engineering and marketing positions. Maniar received his M.B.A from Santa Clara University, his M.E. from University of South Carolina and his B.E. from University of Bombay, India. He is an active member of the TiE (The Indus Entrepreneurs) Semiconductor special interest group.