cadence®

Encounter Conformal Equivalence Checker

Formal verification technology for fast and accurate bug detection and correction

Cadence® Encounter® Conformal® Equivalence Checker (EC) makes it possible to verify and debug multi-million–gate designs without using test vectors. It offers the industry's only complete equivalence checking solution for verifying SoC designs—from RTL to final LVS netlist (SPICE)—as well as FPGA designs. Encounter Conformal EC enables designers to verify the widest variety of circuits, including complex arithmetic logic, datapaths, memories, and custom logic.

Encounter Conformal EC

Already proven in thousands of tapeouts, Encounter Conformal EC is the industry's most widely supported independent equivalence checking product. It is production-proven on more physical design closure products, advanced synthesis software, ASIC libraries, and IP cores than any other formal verification technology.

Encounter Conformal EC is available in three configurations: the L offering delivers core equivalence checking technology; the XL offering extends the L capabilities with automated checking of complex datapaths and equivalence checking of the final place-and-route netlist; the GXL offering extends the L and XL capabilities with transistor circuit analysis for custom designs and embedded memories.

Engineers can use the GXL offering with custom embedded memories, arithmetic blocks, datapaths, standard and extended libraries, and all other custom and semi-custom digital circuit functions. Circuit styles supported include standard and complex Boolean functions, latches and registers, pass-gate, transmission-gate, tri-state switch logic, pre-charged logic cells, domino logic blocks, and dual-rail.

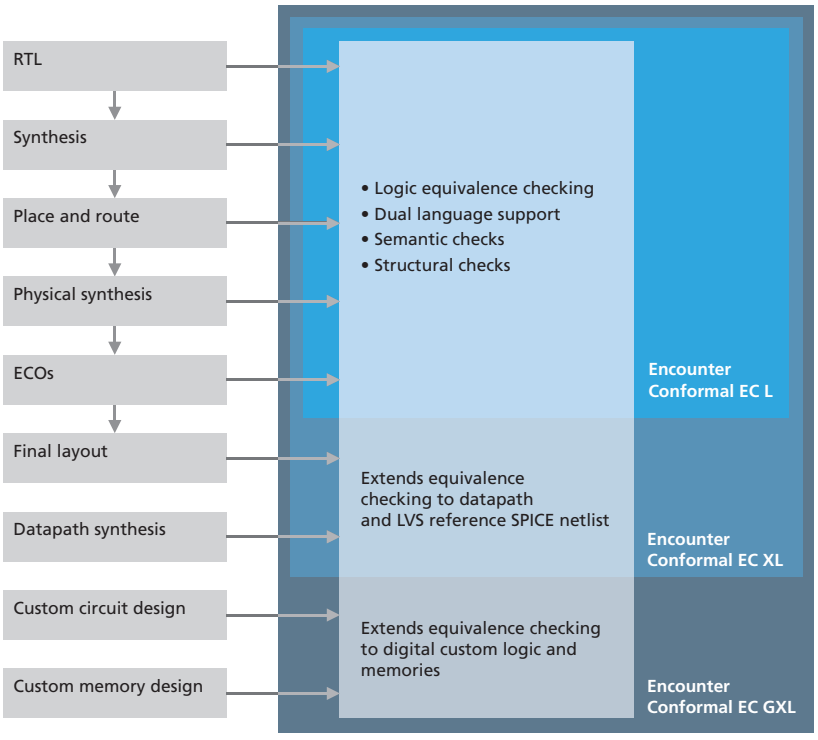

Figure 1: Encounter Conformal EC offers a complete solution, from RTL to final layout, to drive convergence on design goals

Benefits

- Exhaustively verifies multi-million–gate ASICs and FPGAs several times faster than traditional gate-level simulation
- Decreases the risk of missing critical bugs with independent verification technology
- Enables faster, more accurate bug detection and correction throughout the entire design flow
- Extends equivalence checking capability to complex datapaths and closes the RTL-to-layout verification gap (XL configuration)
- Ensures RTL models perform the same functions as the corresponding transistor circuits implemented on silicon (GXL configuration)

Features

Conformal Equivalence Checker L

Equivalence checking

During a design's development, it undergoes numerous iterations prior to final layout, and each step in this process has the potential to introduce logical bugs. Conformal EC L checks the functional equivalence of different versions of a design at these various stages and enables designers to identify and correct errors as soon as they are introduced, thereby maintaining the initial design intent.

Design flow independence

Conformal EC L provides an independent audit of the design process to eliminate the risks associated with sharing technologies across design implementation and verification products. The tool includes technologies developed independently from the design flow, such as production-proven HDL parsing, synthesis, mapping, optimization, and datapath algorithms. Using Conformal EC L ensures that you will catch the maximum number of design bugs.

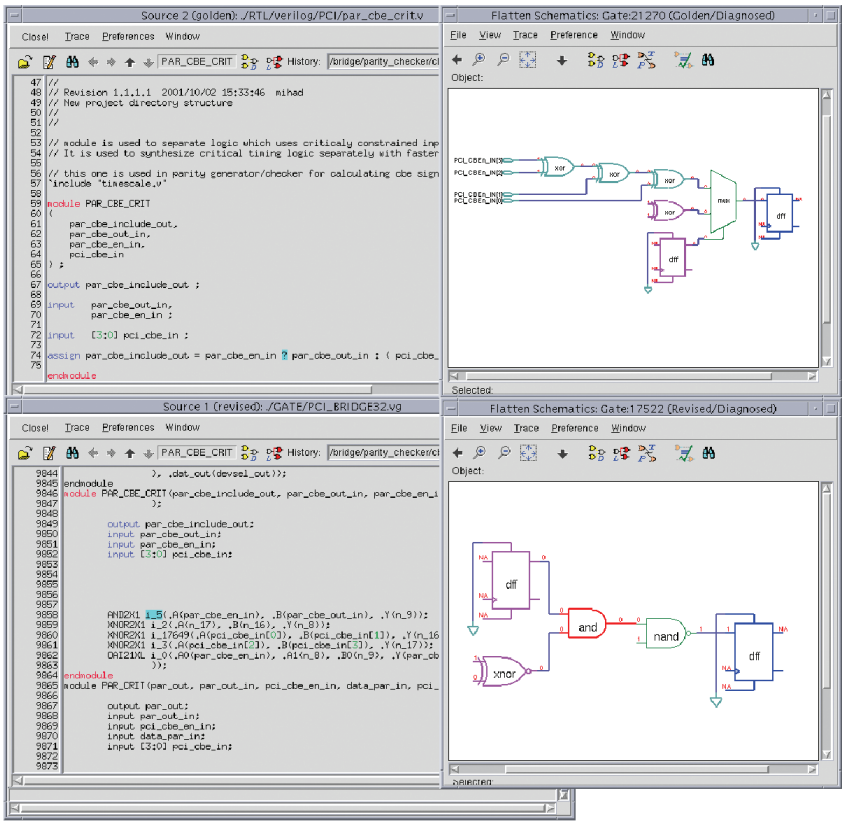

Figure 2: Encounter Conformal EC has an easy-to-use GUI with extensive diagnosis and debugging capabilities

Integrated environment

An intuitive GUI provides for setup and debugging, allowing you to work more productively and quickly pinpoint the cause of mismatches:

- Graphical debugging via an integrated schematic viewer that shows logic values for each error vector
- Full cross-highlighting between RTL model and circuit
- Automatic error candidate identification with assigned and weighted percentages
- Logic-cone pruning to focus debugging on relevant information

FPGA equivalence checking support

As FPGA devices continue to grow in size and complexity, FPGA designers are facing design closure challenges similar to those encountered by their ASIC counterparts. Equivalence checking has become a necessity in the FPGA design implementation flow. Conformal EC L supports Synplify Pro synthesis, as well as the Xilinx ISE and Altera Quartus II implementation flows.

Conformal Equivalence Checker XL

Datapath synthesis verification

Datapath optimization can create designs that are difficult to formally verify because of complex arithmetic operations. Designers have been relying on simulation to verify datapath blocks, but simulation runtimes are exceedingly long and the results can be incomplete.

Conformal EC XL offers a first-of-its-kind formal solution that exhaustively verifies complex datapath blocks without using test vectors. It can handle a wide variety of datapath structures required for high-performance designs:

- Automatic flat datapath module verification—Enables easy verification without manually specifying boundaries or architectures in the flattened netlist; automatically verifies merged operators; compares circuitry that has gone through expression optimization and automatically verifies multipliers with standard architectures and dynamic structures
- Advanced pipelining check and diagnosis—Verifies proper implementation of pipelined designs
- Carry-save verification capability—Allows verification of circuits containing carry-save transformations introduced during optimization for sequence of adders, multipliers, and registers

Final circuit verification

Conformal EC XL is the only verification product that enables a complete verification solution from RTL to final layout, driving convergence on original design goals. It functionally compares a SPICE netlist created for LVS or extracted from GDS to the RTL or gate model. This process ensures that the circuit on silicon has the same intent as the initial design that was verified.

Smart setup and diagnosis

Conformal EC XL includes a set of intelligent analysis commands to ease setup and diagnosis. For example, smart setup investigates the current environment and automatically remedies common setup issues sometimes experienced by new users. In tandem, non-equivalent analysis can be invoked if non-equivalences are encountered, and presents concise root cause information for quicker debug.

Parallel processing

For larger and complex designs, overall verification time can be reduced with multiple licenses by running comparison and datapath analysis on many machines or cores simultaneously. LSF is also supported.

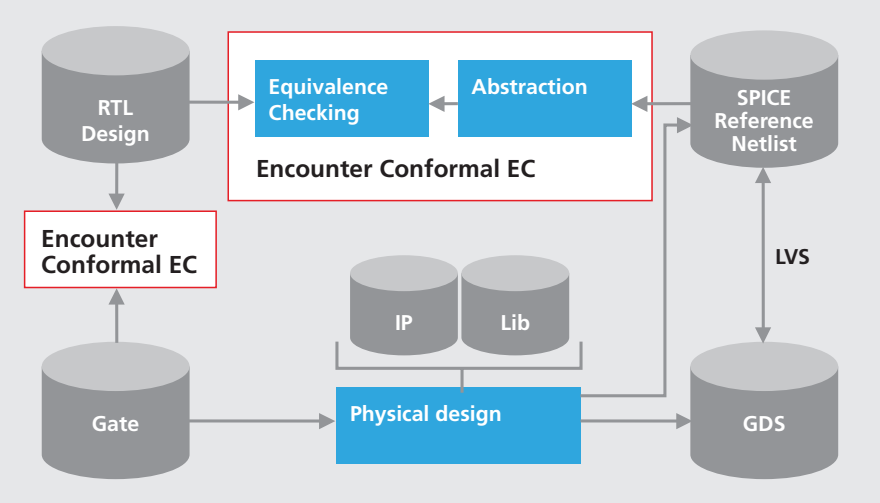

Figure 3: Encounter Conformal EC provides complete verification from RTL to SPICE

Conformal Equivalence Checker GXL

Custom logic abstraction

Conformal EC GXL analyzes digital transistor circuits and abstracts an equivalent logical Verilog model. The underlying abstraction algorithms are more powerful than pattern-based solutions. A Verilog gate logic model of the abstracted circuit can be used for:

- Equivalence checking
- Fault grading—Preserves the circuit hierarchy and structure for maximum debugging efficiency
- Emulation—Provides accurate emulation models for actual transistor-level circuits
- Simulation acceleration—Runs many times faster than SPICE circuit simulation

Memory verification

Traditional and symbolic simulation tools do not scale for verifying today's memory functions and their ever-increasing complexity. Conformal EC GXL provides exhaustive logic verification and— since no testbench is needed—the quality of results is not limited by availability of time or resources to develop comprehensive tests. Conformal EC GXL generates memory primitive models for Verilog system simulation and complete logic function verification of the transistor circuit design using abstraction and equivalence checking.

- Intuitive graphical interface to generate specific primitives
- Generated primitives are address, word, and column MUX-configurable
- All read-write, read-only, and write-only combinations can be generated
- Generated simulation models have the highest performance and contain built-in assertions for trapping illegal memory use such as address collision and simultaneous read-write

Encounter Conformal Technology

To shorten overall design-cycle times and minimize silicon re-spins, designers need production-proven validation. Encounter Conformal verification technologies offer the most comprehensive and trusted solutions for equivalence checking, timing constraints management, asynchronous clock-domain-crossing synchronization checks, functional ECO analysis and generation, and low-power design verification.

The Encounter Conformal technology family consists of Conformal Constraint Designer, Conformal Equivalence Checker, Conformal Low Power, and Conformal ECO Designer.

Platforms

- Linux (32-bit, 64-bit)
- Sun Solaris (64-bit)
- IBM AIX (64-bit)

Language Support

- Verilog (1995, 2001, 2005)
- SystemVerilog
- VHDL (87, 93)
- SPICE (traditional, LVS)
- EDIF
- Liberty
- Mixed languages

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- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
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