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Interview: Learn to Optimize Your Low Power Design Process

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Interview with Neil Hand, Cadence: Learn to Optimize Your Low Power Design Process

ECN Design Network, which features ideas, tips, and tutorials for the electronic design professional, is featuring a series of tutorials on low power design to address an issue of interest to many of its readers. Cadence is participating with a series of tutorials on the subject. To get a preview, cdnusers talked to Neil Hand, Cadence Vertical Solutions Marketing director.

cdnusers: Tell us about the ECN Design Network low power tutorials.

Neil: The tutorials were created to help designers and engineers who are interested in optimizing their low power design process. The first of the four-part series deals with start-up considerations. It applies to design and verification engineers as well as to managers who want to understand what they need to know to get things in place for the design team.

It answers many questions that people getting started in low power design ask. What will I gain by using low power techniques? If I use low power techniques, what impact will it have on my design flow? What do I need to ask my vendors? What do I need to ask my EDA providers?

cdnusers: What about the following three tutorials?

Neil: Each of the others deals with a different area of the design process. The second deals with the front-end design portion. How do you capture an RTL design that deals with low power? How do you go through synthesis, making sure to capture all design intent correctly?

The third deals with verification challenges. How do you verify low power intent? This is important, because as we add low power to a design, we actually change the way the design behaves, and we need to verify those behaviors.

The fourth tutorial looks at digital implementation itself. We discuss physical implementation and power grid signoff. We help designers and engineers see how different low power techniques affect that process.

cdnusers: Let's talk about the first in the series.

Neil:The first tutorial gives an overview of the business and the technical challenges that lead designers to look at low power design. It helps engineers understand what makes up power consumption in a design. They will learn the difference between leakage power and dynamic power

and understand how their process is impacted by different power control techniques.

By using power shutoff and multi-supply voltages and dynamic frequency voltage scaling as examples, we give an overview of power control techniques such as clock gating and multiple voltages. Then, we look at the impact of those techniques on the methodologies that we have in our design flows today.

From there, we look at some of the more practical considerations. For example, if we are going to implement power shutoff, what do we need to ask our vendors and our software tool providers to make sure we do not get ourselves into a hole that we have to dig ourselves out of later in the design?

Why do we address all these questions? Because we find many people dive into low power without knowing the full implications of what they are trying to do. And, as a result, it becomes a much bigger challenge than they realized.

cdnusers: It sounds as if it is not simply a matter of implementing a few power saving techniques.
Neil:True. There are larger considerations. Implementing a technique and capturing it in the design is only one challenge—making sure you have done it correctly and that you can take it all the way through to manufacturing is another.

cdnusers: There are a lot of different applications out there. Can a basic tutorial address them all?
Neil: Techniques vary widely depending on the target application. Some designers are able to meet their goals simply by using automated techniques such as automatic clock gating and multi-threshold voltage libraries. But once you start needing more aggressive types of power saving, you need to look at the more advanced techniques such as multiple supply voltage and power shutoff.

For example, if you have a design, like a mobile handset, large portions of it are not always active. In these types of designs, we can use power shutoff and save a considerable amount of power. But, if you have a design where everything is always running at full speed, and needs to always be at full speed, we may have to look at techniques like multiple supply voltage or a combination of those techniques. So, different techniques are needed for different applications.

And that's at the simplest. You can have a combination of all of them in the form of dynamic frequency involved scaling, where we dynamically adjust the design to meet just the requirements that we have at that time.

cdnusers: This sounds very complicated. You clearly are covering a lot of material. How long is this tutorial, how in-depth can you go in a tutorial?
Neil: The tutorials themselves are short so engineers can digest them easily. They are only about 15 minutes in length. The aim is to provide an overview of the subject matter—to give someone

enough information that they know what questions to ask. We can follow up with extremely in-depth information for those who are interested. There is more information on this site and on the cadence.com Web site. Users can also attend Cadence techtorials and workshops about low power design that allow them to get a much deeper understanding of the process.

cdnusers: You mentioned mobile handsets earlier. Are these tutorials directed at wireless designers exclusively, or do they have broader appeal to semiconductor designers in general?
Neil: The tutorials and the challenges they cover apply to anyone who has to deal with power efficient designs. It is broadly applicable to designers who are looking at power for the purpose of reducing costs, or to enable a high degree of performance, or a high degree of integration. They apply to anyone who wants to reduce cost by reducing the cooling and the packaging requirements for a device. It's important to remember, that by using low power techniques, you can help alleviate the cost of production.

Additional Information About the Tutorials
The first tutorial, Practical Considerations for Low Power Design, is available now. The remaining three will be presented over the next few months.

The second tutorial, Low Power RTL Design, focuses on how low power affects every aspect of the RTL design process from coding through synthesis and DFT. The tutorial looks at how coding style can impact low power design, how to capture power intent using the Common Power Format (CPF), and how synthesis and DFT are impacted by low-power design. Also discussed are power estimation techniques that, together with CPF, can be used to trade-off different low-power designs.

The third tutorial, Low Power Physical Implementation, discusses why, during physical implementation, designers need to ensure that the power intent of the design is correctly preserved and implemented. This tutorial covers what is required during power planning, the requirements of a low power floor plan, and what needs to be considered when implementing PSO and MSV during physical design. Finally, the requirements and challenges in archiving signal integrity and timing closure are discussed.

The fourth tutorial, Low Power Verification, addresses the new verification challenges that low power design introduces throughout the flow entire flow. It covers RTL, netlist, and physical. It looks at the specific challenges of verifying Power Shut-Off (PSO) and Multiple Supply Voltage (MSV)—both functionally and implementation. Using PSO as an example, we see what needs to be done to ensure that PSO does not impact functionality; that isolation and retention are inserted correctly during implementation; and that the final power grid implementation can handle dynamic switching of the power supplies.

For more information:
Cadence Low-Power Solution

Low power Technology zone Cadence User Community

Low power Forum

ECN Design Network

About the author

Neil Hand is a member of Cadence's Vertical Solutions Marketing group focusing on the impacts of low power on digital design especially as it relates to the wireless and communication market segments. He has over 17 years experience in engineering design, customer support, sales and marketing in industry-leading EDA companies including Cadence, Mentor/0-In, Averant, Get2Chip, and Synopsys. Before working in design and verification, he was a telecommunications design expert at Ericsson. Neil holds Bachelor of Electrical Engineering and Bachelor of Science Computing degrees from the Queensland University of Technology in Australia.