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Interview: Advanced Low-power Techniques to Mitigate Headaches

From cdnusers.org on 29 January 2007

The community interviewed Sean Huang to better understand how Omnivision uses advanced low-power techniques to design their chips.

cdnusers: Sean, first tell us about Omnivision

Sean: OmniVision designs and markets high-performance semiconductor image sensors. Our OmniPixel® and CameraChipTM products are highly integrated single-chip CMOS image sensors for mass-market consumer and commercial applications such as mobile phones, digital still cameras, security and surveillance systems, interactive video games, PCs and automotive imaging systems. OmniVision also designs ASIC chips as the camera bridge to provide application solutions for customers.

cdnusers: Why is low-power design important for you?

Sean: Our chip's application is mainly for mobile devices which are expected to have longer battery life. Additionally, increasing functionality, performance and integration within our chip is leading to power-consumed designs. So how to make the chip lower power is very important for our company.

cdnusers: What do you find are the drivers of low-power?

Sean: Advanced technology is a critical driver. New electronic products require more function, high performance and big volumes with low cost per unit, so accordingly they require advanced process generation such as 90nm and below, which have much higher power consumption not only in leakage power, but also higher dynamic power density than previous process. Those will boost low-power chip design.

cdnusers: Why do you use advanced low-power techniques such as MSV/PSO?

Sean: Power management is a big concern for us, no matter whether in terms of switching power, or leakage power. Multiple supply voltage (MSV) and clock-gating will help our chip to save dynamic power during operating mode; Power-shut-off (PSO) and High-vt cells will reduce leakage current in our chip during stand-by mode.

cdnusers: Have you used any of these techniques in your chip?

Sean: Yes, we adopted those low-power techniques in our ASIC chip, such as: several analog power domain, 2 voltage islands for digital, power-shut-off technique, most High-vt cells, different-level clock gating, IR drop and EM analysis etc. Now we are using these techniques in our image sensor

chip.

cdnusers: Why did you not use these techniques in the past designs?
Sean: We used the 0.18um process for most of our previous designs which are not so complicated in functionality, thus power was not a big issue at that time. But things are always changing: now power consumption is headache for us.

cdnusers: How did you do your power analysis for these techniques?
Sean: We used VoltageStorm Professional Edition(VSPE) to analyze the integrity of the power grid to ensure its robustness in our design, and also we used VoltageStorm Dynamic Gate(VSDG) to analyze the effect of simultaneous switching activity which could cause transient IR drop failures. Both tools work closely with First Encounter and CelticNDC as our timing, power and SI closure flow.

cdnusers: Will you be using advanced low-power techniques in the future?
Sean: Definitely. We need to design our chips with high performance, low cost and low power to meet our customers' requirements. To achieve this goal, it is a necessary step to use those advanced low-power techniques in our design. I think in the future we will explore more low-power techniques, such as MTCMOS, state retention power gating, back bias, DVFS etc.

cdnusers: What is your opinion of Cadence support for these techniques including synthesis, verification, implementation and analysis?
Sean: Cadence Encounter® platform provides a complete low-power solution, such as single pass concurrent power, timing and area optimization in RC, and complete MSV support & accurate MSV signoff with power, timing, SI analysis and IR Drop in SoC Encounter.

cdnusers: Did Cadence tools help the current design for these techniques?
Sean:We implemented those advanced low-power techniques in our chip without too much pain: no bottom-up synthesis, no separate P&R and timing/SI analysis for different power-domain, no manual floating check between different power-domain, etc. And we explored the low-power design flow without changing our previous design flow a lot. With Cadence tools help, we were able to concentrate more on the design itself, not design flow.

cdnusers: How did you find Cadence tools for solving these challenges?
Sean: We did a lot of research about low-power techniques according to our foundry TSMC reference flow. Cadence Encounter platform uniquely addresses the above challenges with automated implementation capability, as well as accurate sign-off analysis capability that could shorten our design cycle. Finally we decided to adopt Cadence low-power solution.

About the author
Sean Huang has worked with OmniVision Technology Inc. in the ASIC Department since 2001. Initially as a design engineer, then as design manager, he is in charge of the physical design flow

and leads the back-end team responsible for the implementation from Netlist to GDSII. He obtained his MSEE in 1999 from the Institute of Microelectronic of Chinese Academy of Sciences, and in 1996 obtained a B.S. in Resource Engineering from the University of Science and Technology, Beijing.