Multigig and Cadence

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Haris Basit, Chief Executive Officer, Multigig

The Customer

Clock technology is a fundamental part of integrated circuit (IC) design and performance, whether it is analog, digital, or mixed signal. Delivering a low-jitter, low-skew timing signal to a large number of elements placed over the whole IC area is becoming increasingly difficult. In traditional clock design, these issues have made clocking a major power drain, consuming more than half of the total power dissipation in some ICs. In many cases, the clock signal is the limiting element in the power distribution design.

Multigig, based in California, is a fabless semiconductor startup that has developed dramatic new advances in low-power, high-performance, mixed-signal chips. The company has developed a revolutionary new clock signal technology that reduces power requirements and yet provides improved performance. Multigig's RotaryWave circuit technology is based on differential transmission lines that circle back on themselves like a Möbius loop.

The RotaryWave design dramatically reduces dynamic power dissipation through recycling the charge—much the way an LC tank does but for much larger loads. By providing multiple access points and automatic synchronization among multiple clocks, this method also eliminates the need for a dedicated distribution mechanism. Together, these factors promise to reduce power requirements associated with the clock signal by 50% to 80%. Multigig has built and tested circuits with hundreds of phases for each clock period, allowing picosecond resolution with reduced phase noise and jitter.

"This clocking technology lets you rethink how to design many circuits, providing a whole new dimension for the architecture," explains Haris Basit, CEO of Multigig.

Business Challenge
- Identify problems early in the process to avoid costly re-spins

Design Challenges
- Simulation of complex RF and mixed-signal designs
- High-frequency, low-amplitude PLLs

Cadence Solutions
- Virtuoso Spectre Circuit Simulator
- Virtuoso Spectre RF Simulation Option
- Virtuoso UltraSim Full-Chip Simulator
- Virtuoso AMS Designer Simulator

Results
- Fast and accurate design and simulation of RF blocks
- Full-chip simulation and verification

The Challenge

This promising new technology does not change the fundamentals of circuit design, but requires layouts that have never been done before. There are no existing EDA systems or design flows that incorporate RotaryWave clock elements, or looping circuit configurations in standard libraries. These design challenges lead to simulation and verification difficulties as well. Multigig found that its existing software platform was unable to simulate these innovative circuit elements.

"In the area of simulation, Multigig faces two very difficult problems: 1) accurate simulation of extremely low phase noise; and 2) full-chip simulation of complex mixed-signal ICs," Basit says. "An error in either can result in extra design iterations—missing critical sales windows."

> *"Together, Virtuoso AMS Designer and Virtuoso UltraSim comprise a verification flow that we are confident will produce functionally correct silicon the first time."*

One of the designs Multigig is working on to prove the capabilities of RotaryWave technology involves a phase-locked loop (PLL) with a complex voltage-controlled oscillator (VCO) that operates at a very high frequency, but with low amplitude. Success in this design requires highly accurate simulation capabilities for unusual configurations. In addition, the design must be verified from the block level, through each level of functionality, all the way to the full-chip level.

The Solution

Cadence engineers collaborated with Multigig to simulate the complex analog-digital circuits using the Cadence® Virtuoso® Spectre® RF Simulation Option.

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Cadence also provided engineering support to Multigig to overcome several obstacles and optimize simulation performance. On the design side, Cadence suggested performing the simulation from various perspectives to identify limiting cases and the phase-locking capability of the PLL. These simulations identified problems early in the process, before they could create costly re-spins.

Full-Chip Verification

Multigig was especially looking for a block-to-full-chip simulation solution for its revolutionary new clock circuit design. Cadence provided Multigig with an integrated design solution from the block level to the fully completed chip with its Virtuoso custom design platform. Multigig used Virtuoso Spectre Circuit Simulator and the Virtuoso Spectre RF Simulation Option at the analog block level, and then Virtuoso UltraSim Full-Chip Simulator (the Cadence implementation of FastSPICE) for verification at the top levels.

"At Multigig, we use Virtuoso UltraSim to perform transistor-level simulations of our top-level design that would not be possible with Virtuoso Spectre technology alone," Basit explains. "While Virtuoso AMS Designer Simulator with Verilog language is faster, Virtuoso UltraSim has an important place in our verification flow because it can prove functional correctness without the abstractions required for the Verilog interface of AMS Designer. Together, Virtuoso AMS Designer and Virtuoso UltraSim comprise a verification flow that we are confident will produce functionally correct silicon the first time."

Flexible Licensing and Up-to-Date Foundry Support

Virtuoso simulation technology gives Multigig the flexibility to use the wide array of Cadence mixed-signal design and verification software as needed. Virtuoso technology's unique token-based implementation allows developers to get access to what they need, when they need it, without the corporate overhead of owning the entire software platform. As Multigig's needs grow, it can simply add more tokens incrementally, without taking a big hit all at once.

Another advantage of the Virtuoso suite is that it provides direct support for the particular foundry process design kit (PDK) that Multigig uses. Multigig had been working with conventional software for radio frequency (RF) and phase noise simulation, but found that it did not always have the latest foundry support. With Virtuoso technology, Multigig is assured that the process from tapeout to fabrication will be smooth and error-free.

Summary

By incorporating Cadence Virtuoso technologies, Multigig design teams benefit from faster, more accurate simulation and verification of high-precision mixed-signal ICs, allowing them to focus their engineering resources on advancing their revolutionary clocking technology in future projects.

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