Full-chip mixed-signal verification using high precision digital-analog interface element

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Organization of Presentation

- **Drawbacks of the current methodology.**
  - Digital simulations using behavioural models.
  - Inaccurate transition time at each input of analog module.
  - Inaccurate interface elements between analog and digital modules.

- **How the problem is solved?**

Organization of Presentation

- **Scope - Case study of Timer modules in a low-power microcontroller.**
  - Block Diagram.
  - Design Database Details.
  - Interface element (Connect Module).
    - Effect of default interface element.
    - Effect of high precision interface element.
- **Results.**
- **Conclusions.**

Drawbacks of the current methodology

- **Digital simulations using behavioural models.**
  - Behavioural models are typically used for the analog modules to be verified in the full-chip context.
  - Typically no internal timing information of analog modules is available during the gate level netlist simulations.
  - Typically timing information for the interconnects between analog and digital modules is not available.
  - If an analog module has to be verified for its functional and timing correctness, there may be a need for standalone testbench to verify the analog-digital interface and requirement for new or modified test vectors.

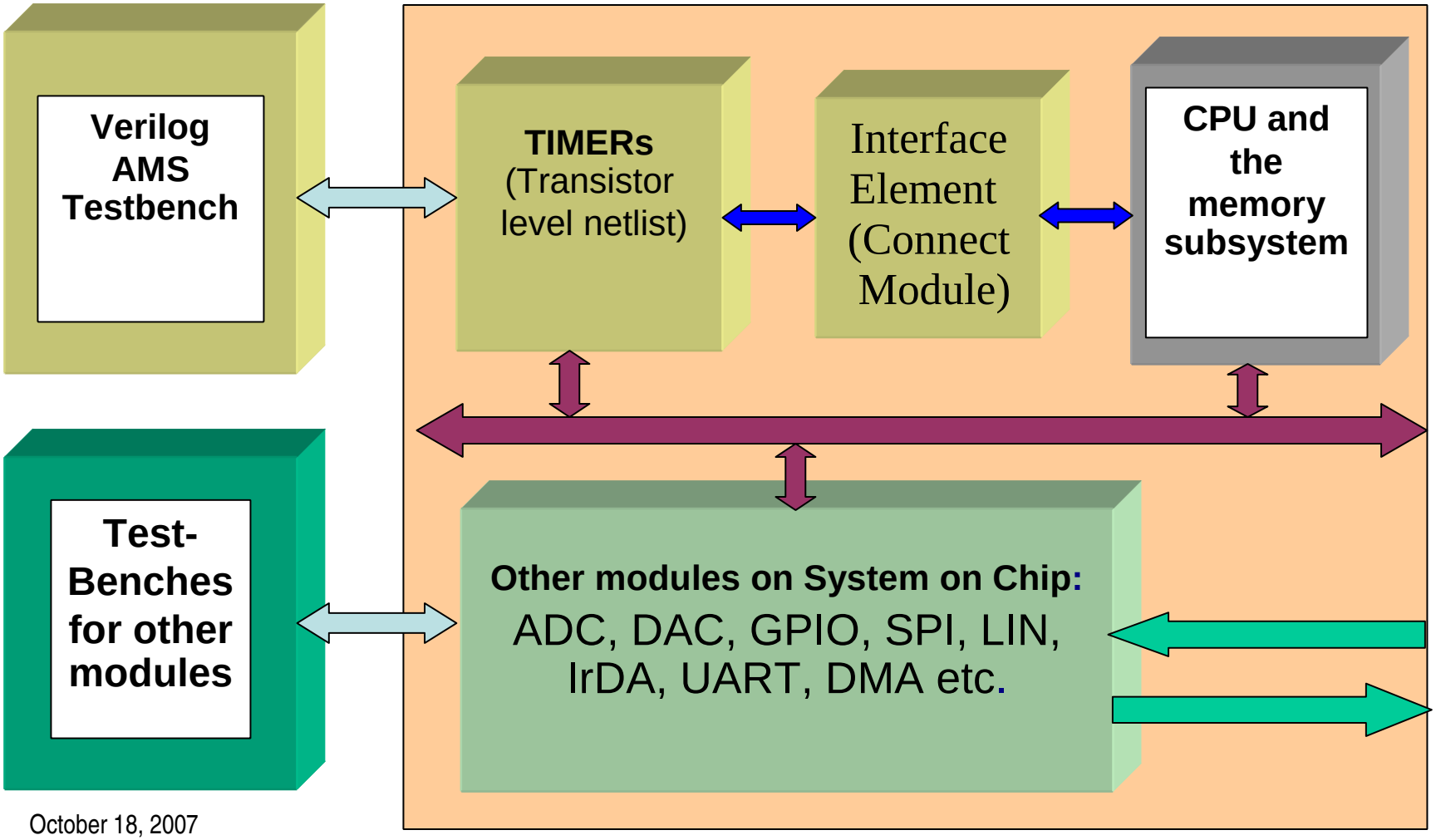
Drawbacks of the current methodology

- **Inaccurate transition time at each input of analog module**
  - Current methodology cannot calculate the input transitions for every input port.
  - This may lead to functional failures in Silicon.

Drawbacks of the current methodology

- **Inaccurate interface elements between analog and digital modules.**
  - No control on input delay at the input ports of analog module.
  - No control on transition time at the input ports of analog module.

System On Chip (SOC)



How the problem is solved?

- **Transistor level netlist is used for analog modules instead of behavioral models.**
  - Accurate transistor models are used in the netlist available for analog module.
  - Accuracy is same as running SPICE simulations.
- **For all the other modules in System On Chip (SOC) , gate level netlists and timing information in Standard Delay Format (SDF) is used.**

How the problem is solved?

- **Existing full-chip digital testbench and functional test vectors can be re-used.**
  - Can be easily extended to other analog modules in SOC like IOs, oscillators etc.
  - One or more analog modules can be simulated together depending on run-time, complexity of simulation vectors etc.

- **Accurate transition time calculation.**
  - Primetime is used to calculate the accurate transition times at each input of the analog module.
  - .lib is created with the input capacitances characterized for these analog modules. RC extracted spice netlist is used for the same.

How the problem is solved?

- **Accurate transition time calculation.**
  - These are read into primetime and the slews and delays are dumped out for all the input pins.
  - For outputs of the timer modules, 20% and 80% rise and fall thresholds are used for analog to digital conversion respectively because the digital library delays are characterized at the same thresholds.
  - Automated setup can read this primetime file and dump out the high precision interface element module which can be simulated.

How the problem is solved?

- **High precision Interface Element used.**
  - Default interface element is not accurate with respect to the transition times of input signals to the analog block.
  - High precision interface element has complete control on transition time and absolute delay of all input signals of analog block.

Scope - Case study of Timer modules

- These timers are used in a low-power microcontroller device.
- Timer modules' correct functionality and accurate timing is extremely critical for the application software. These are used for capturing external events and generating PWM (pulse width modulated waveform) outputs.

Scope - Case study of Timer modules

- **Proposed flow executed on one Timer with 3 capture and compare channels and second Timer with 7 capture and compare channels.**
  - Both the modules mentioned above are Analog Modules with the logic in the transistor level netlist form (No standard cells from the timing characterized libraries are used).

Scope - Case study of Timer modules

- Verify functionality and timing for the above mentioned modules in the system level context.

Scope - Case study of Timer modules

- **Design Database Details**
  - All the digital modules in the form of gate level netlists with the timing information available in Standard Delay Format (SDF) file.
    - All the modules in SOC are instantiated at Design Under Verification (DUV) level called “duv”. This is top level Verilog Netlist.
  - Other non-critical analog modules in behavioural form.
  - Both Timer’s in transistor level netlist (SPECTRE format).
  - Timer modules’ input port capacitance values dumped by running Spice simulations (negligible runtime overhead).

Scope - Case study of Timer modules

- **Design Database Details.**
  - There are a few test-benches around the SOC to cater to the verification of other modules.
    - E.g. Clock generation, Memory loaders, Serial peripheral controllers etc.
  - This whole system is simulated using the simulator Nc-SIM (From Cadence) which in-turn invokes AMS-Ultra (Simulator from Cadence) for simulating Timers.

Scope - Case study of Timer modules

Interface Element (Connect Module)

- **Default Interface Element:**
  - Apply same transition time to all ports of analog module.
  - Same value for rise and fall transition which adds to inaccuracy.
  - Timer interrupts asserted correctly in mixed-signal simulation, but Silicon showed functional failure where interrupts were lost (refer Figure 1).
  - Accurate design fix is not possible since the failure could not be simulated.

Scope - Case study of Timer modules

Interface Element (Connect Module)

- **High Precision Interface Element:**
  - Highly accurate rise and fall transition time for all input ports of analog module.
  - Highly accurate rise and fall delay for all input ports of analog module.
  - Timer interrupts NOT asserted in simulation and behaviour was correlating with failure results seen on Silicon (refer Figure 2).
  - Accurate fix of design database was possible since failure could be simulated and fix could be qualified.

Effect of Default Interface element

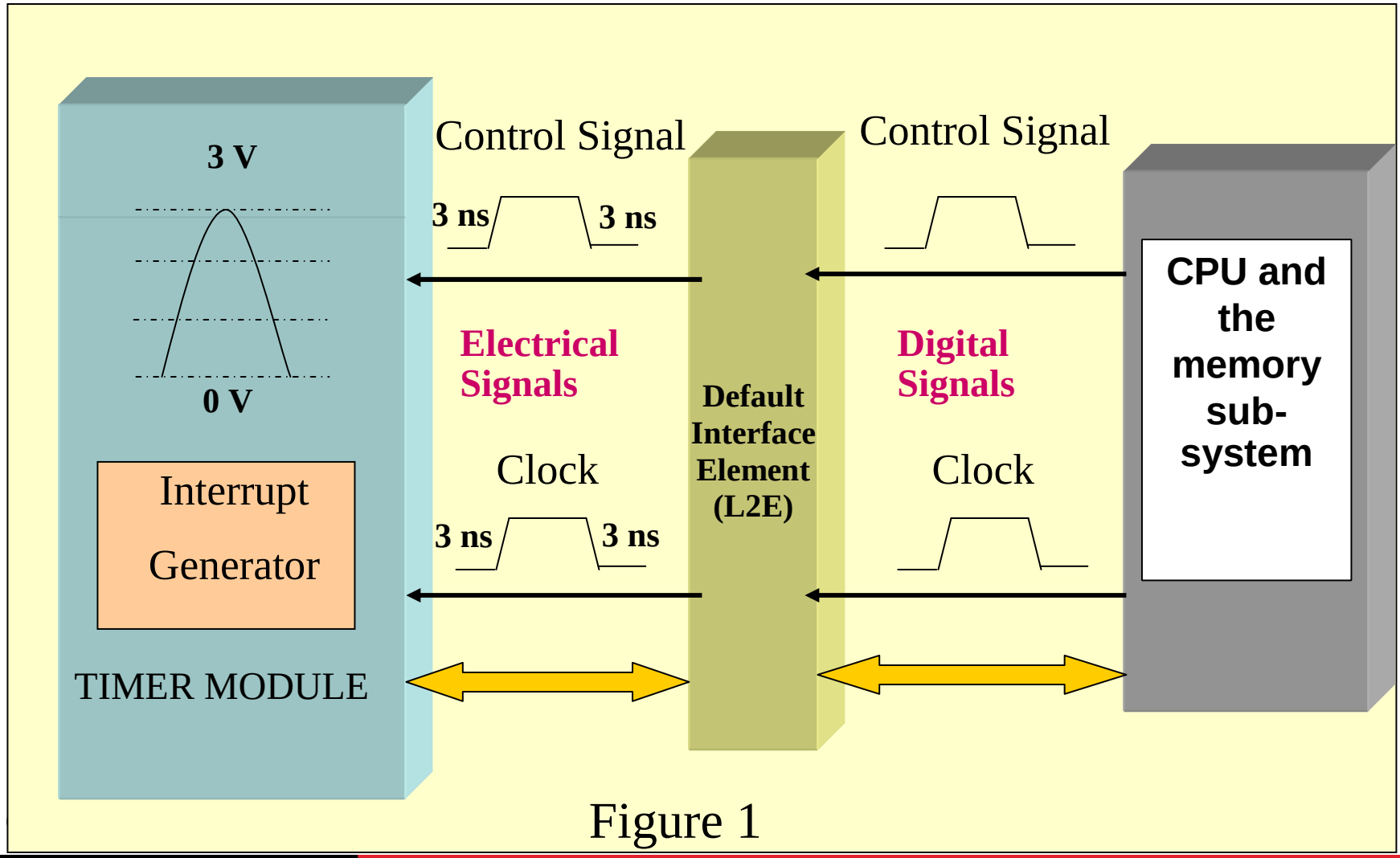


Figure 1

Effect of High Precision Interface element

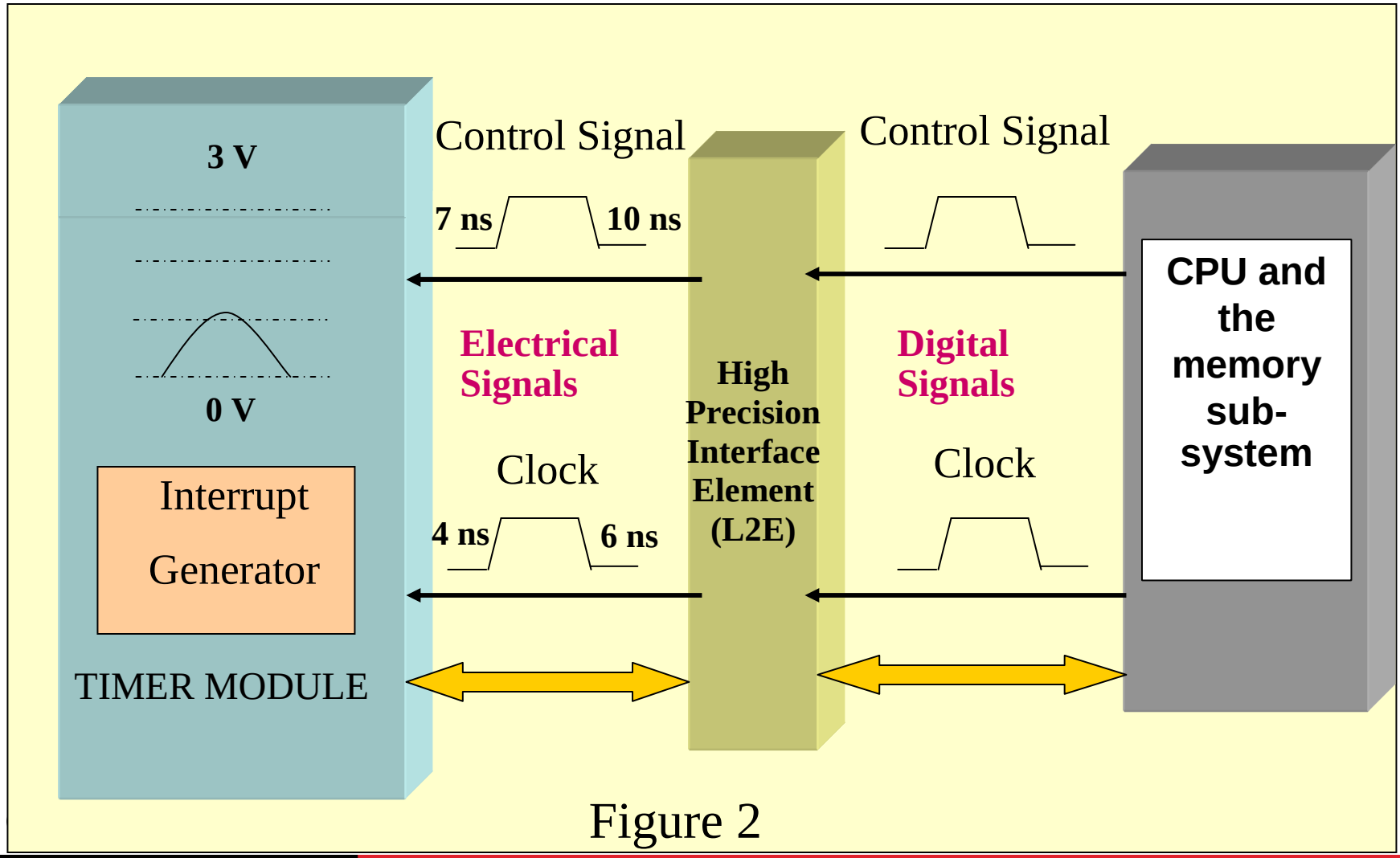
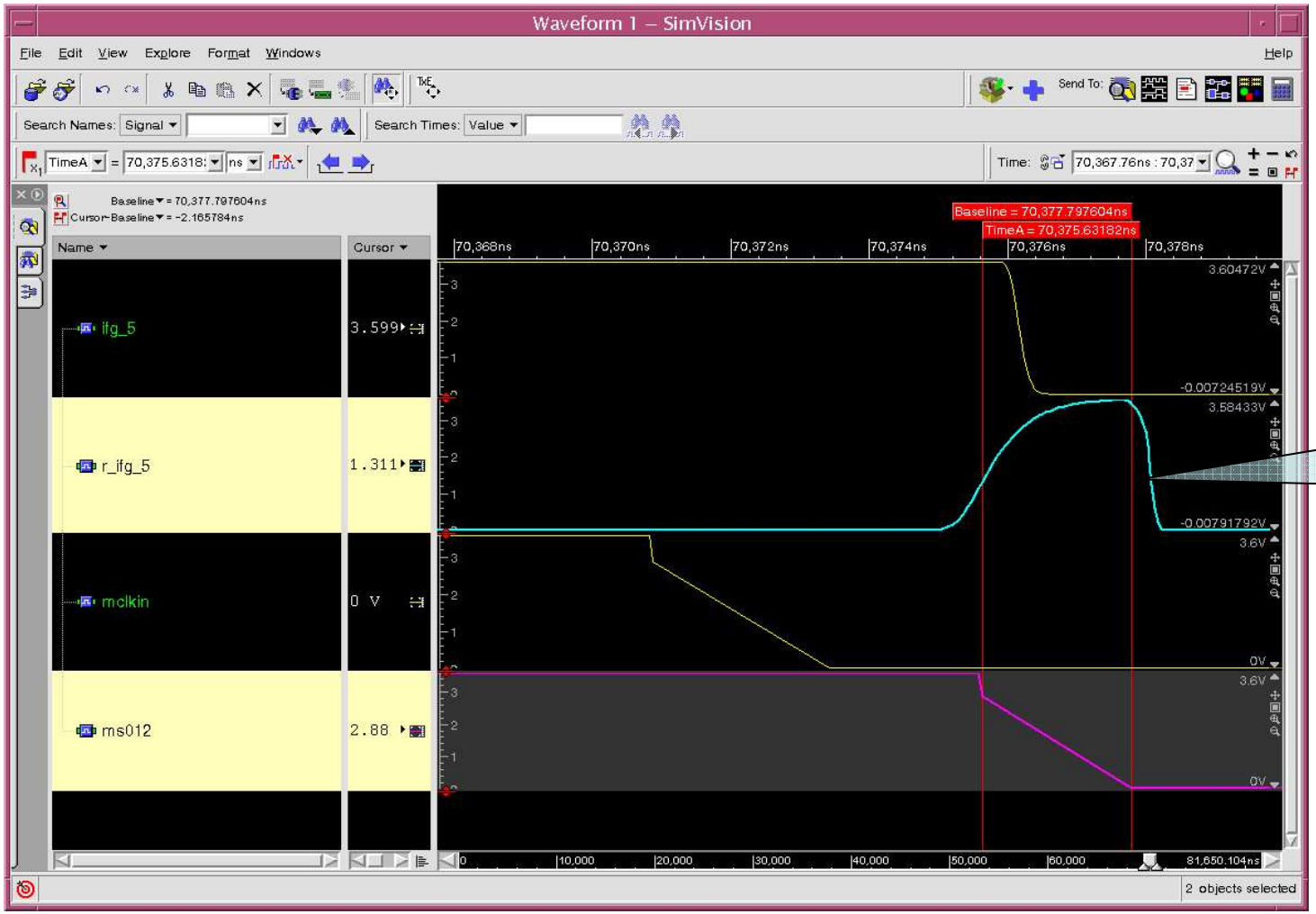


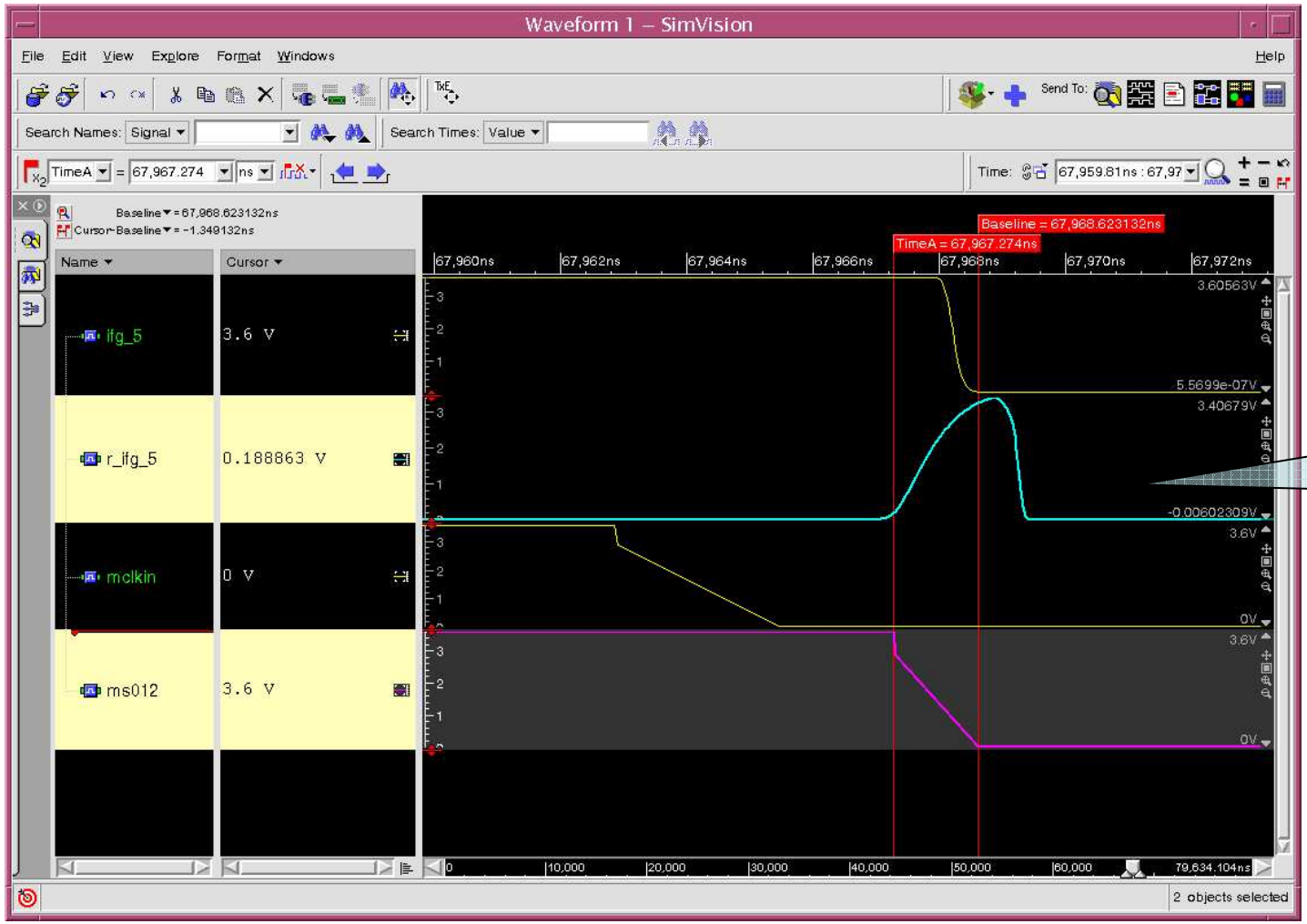
Figure 2

Simulation output in simvision



Tr = 2.2ns
Pulse width = 2ns

Simulation output in simvision



Tr = 1.3ns
Pulse width = 1.2ns

Results

- All the existing tests for both Timers are verified using the high precision interface element.
- Timer interrupt issue seen on first silicon fixed in design database and qualified successfully on latest Silicon.
- All tests are passing in the new verification flow proposed in this paper.

Conclusions

- This flow can be easily ported across other designs using Cadence's simulation environment.
- Including more analog modules in transistor format for simulations easily possible (at the expense of increased runtimes).
- Since these modules must be used in all the future devices as is, this methodology guarantees the correct module behaviour in Silicon.

Future scope

- Signal transition in high precision interface element is assumed to be linear. There may also be non-linear. Analysis should be done to check the effects of non-linearity.
- 0-20% rise and 100-80% fall transition could not be made as a step transition. Different way has to be thought about correcting this.