# ACCELERATING ANALOG SIMULATION WITH FULL SPICE ACCURACY



## INTRODUCTION

Advanced process technologies and modern integrated circuit (IC) designs with complex design metrics and standards have turned analog and RF simulations into multi-day or multi-week engineering tasks. As a result, the need for a holistic and optimized simulation solution that incorporates analog, RF, and AMS has become more pressing and widespread. This is especially true in cutting-edge low-power, low-noise designs at 90nm and below. However, it is by no means a problem exclusive to such process nodes. The resulting simulation performance bottleneck has increasingly strained IC designers' productivity and their products' time-to-market schedule.

Ever since the emergence of commercial SPICE simulation tools in the early 1980s, simulation performance has been the driving force for major simulation technology developments. RF simulation technologies take advantage of the periodic steady-state nature of RF designs and provide significant speed-up compared to brute-force transient analysis. FastSPICE explores the hierarchical structure of full-chip design and takes a divide-and-conquer approach to ensure full-chip verification can be done in a reasonable timeframe. AMS encourages a top-down design methodology that mixes much simpler behavioral models with full accuracy transistor blocks to speed-up transient analyses during both design and verification.

This paper focuses on block-level circuit simulation, where today's analog and RF designers demand a 5-10x simulation time speed-up with minimal or no accuracy loss. The overall goal is to significantly increase design productivity by completing a week-long simulation session within the same working day, or a day-long simulation session within a few hours.

## OVERVIEW

Cadence<sup>®</sup> Spectre<sup>®</sup> turbo technology was created to address the simulation and analog verification requirements of modern designs. It is built upon the production-proven analog simulation platform, the Cadence Virtuoso<sup>®</sup> Spectre Circuit Simulator.

The Spectre simulator is widely acknowledged as the industry-standard sign-off simulator with particular strengths being: accurate and robust transient analyses, DC convergence, a complete set of advanced features, and comprehensive foundry and PDK support. Spectre technology is production-proven through numerous silicon tapeouts by many customers, in all market segments, with all process technologies, over the past decade.

While the simulator itself has existed for more than 10 years, it has continuously been at the leading edge of circuit simulation innovation, as evidenced by the development of RF analyses, Verilog®-A behavioral modeling, statistical analysis, and AMS capabilities.

Spectre turbo technology is the next logical evolution in the Cadence analog simulation offering. Improving designer productivity has always been the goal; however, prior enhancements, including those listed above, have largely focused on improving functionality, stability, usability, and performance of particular design types.

### VALUE

Spectre turbo technology improves productivity by drastically reducing simulation time, while still achieving the same Spectre accuracy. Turbo technology has been demonstrated to deliver a **5–10x performance speed-up** for most applications with full Spectre accuracy.

For **large parasitic-dominant designs**, Spectre turbo technology provides a parasitic reduction capability that can significantly speed-up simulation by 10–20x. Without turbo technology, such designs could not have been simulated in a reasonable timeframe.

## TURBO TECHNOLOGY

As is to be expected, there is no single contributor to the performance improvements that Spectre turbo technology provides customers. Instead, many improvements made to the analog simulation engine contribute to the overall performance gain. The main improvements can be categorized under the following areas:

- Multi-rate technology
- Matrix-solving optimizations
- Parasitic reduction
- Iteration reduction
- Enhanced liberal mode
- Full Spectre accuracy

#### MULTI-RATE TECHNOLOGY

The reason that many modern designs take a long time to simulate is that they contain blocks with wide ranges of time constants. As a result, time steps must be very small to capture the small time constants (or high-frequency poles), and the transient analysis period is long to ensure that it covers the large time constants.

Spectre turbo technology contains advanced numerical algorithms that take advantage of the inherent multi-rate behavior of these circuits.

In addition, Spectre turbo technology dramatically reduces the cost of device evaluation, which has traditionally accounted for ~80% of transient simulation time. It achieves this through the use of multi-rate numerical techniques and by more efficiently utilizing modern multi-core CPU architectures.

Turbo technology further reduces the cost of device evaluation via careful re-implementation of device models to remove unneeded and inefficient operations.

#### MATRIX-SOLVING OPTIMIZATIONS

In general, matrix-solve operations will account for 10-20% of simulation time. However, there are some situations where matrix solve can consume anywhere from 50-90% of simulation time. By reducing the cost of device evaluation using multi-rate numerical techniques, the relative cost of the matrix-solve operation will further increase.

Spectre turbo technology improves the efficiency of the matrix package; however it also addresses some specific issues that have been found to dramatically impact performance.

One improvement is in the area of Newton convergence. The cost of matrix solving increases dramatically when matrix re-ordering occurs. The usual causes of this are poorly written behavioral models and a wide dynamic range of entries in the matrix. Spectre turbo technology automatically resolves these issues, and has implemented new algorithms to improve Newton convergence and reduce the occurrence of these situations.

#### PARASITIC REDUCTION

Another area where the cost of matrix solving is prohibitively large is for large parasitic-dominant circuits.

Parasitic reduction can significantly speed-up post-layout simulation, where the amount of parasitics can be as high as 100x or more that of active devices. In these cases, matrix solving dominates total simulation time.

Spectre turbo technology delivers parasitic reduction capabilities that result in a speed-up of up to 50x for parasitic-dominant cases.

Unlike other turbo technologies, parasitic reduction does have an associated impact on accuracy, and it is necessary for designers to understand the tradeoff between accuracy and performance for parasitic reduction.

#### **ITERATION REDUCTION**

For existing Spectre customers, accuracy is traditionally controlled via a single transient analysis parameter: errpreset. Spectre turbo technology provides three pre-defined accuracy levels: the relaxed liberal mode, default moderate mode, and tight conservative mode.

In Spectre turbo technology, the time-step control algorithm has been retuned to reduce the number of Newton rejects in liberal mode and reduce the incidence of unnecessarily small time steps in conservative mode. For particularly challenging cases, this can lead to a significant reduction in the number of overall iterations required.

#### ENHANCED LIBERAL MODE

Spectre Circuit Simulator has always been acknowledged as the industry leader in terms of the accuracy of its simulation results and simplicity of its use model. The errpreset option, with its three possible settings of liberal, moderate and conservative, provides a simple way to trade-off simulation accuracy for performance. In our experience this satisfies the vast majority of designer needs, without requiring further tuning.

The "moderate" errpreset is the default. For high-resolution simulation applications, the user can choose to use the "conservative" errpreset, which typically incurs a 2-3X performance penalty. For simulation applications or verification tasks that do not need as accurate simulation, a user can choose the "liberal" errpreset, which can be 2X faster.

As part of Spectre turbo technology, we have focused on further improving the accuracy of liberal errpreset mode, thus increasing its applicability. As a result, "liberal" errpreset in turbo mode can be safely used for a greater variety of circuits and designers can see additional speedups compared to their typical baseline "moderate" errpreset simulation.

#### FULL SPECTRE ACCURACY

Unlike other approaches, Spectre turbo technology makes no fundamental assumptions about the actual design being simulated. Any such assumptions have invariably proven to be difficult to enforce in real-life circuits, leading to usability and accuracy issues.

Spectre turbo technology does not use any FastSPICE-type approximations such as table modeling, MOS circuit partitioning, or event-driven simulation algorithms. Just as in the standard Spectre simulator, Spectre turbo technology uses the same device equations and solves the entire circuit at each Newton iteration.

## TARGET APPLICATIONS

Spectre turbo technology addresses a broad class of analog circuits and analog subsystem designs across various application types. While not being limited to a particular set of circuits, customers have noted that the following set of circuit types are particularly challenging to simulate, and turbo technology has been proven to be particularly effective achieved with their simulation. *Figure 1* shows a distribution of performance improvements for Spectre turbo technology across a representative set of customer designs.

- PLL, VCO
- Transceivers and tuners
- Data converters
- Power management circuits (DC-DC converters)
- Parasitic-dominant circuits

Distribution of Spectre "turbo" performance

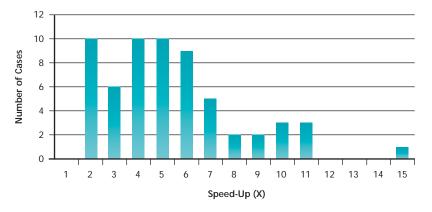


Figure 1: Distribution of performance improvements for Spectre turbo technology over a representative set of customer designs

## A COMPLETE SIMULATION SOLUTION

Spectre turbo technology is an integral part of the Virtuoso Multi-Mode Simulation solution for analog/mixed-signal verification. With turbo technology, designers continue to have access to the different simulation technologies needed for their specific design style and the full breadth of integrations that Spectre technology supports today. Virtuoso UltraSim Full-Chip Simulator provides a FastSPICE simulation capability and Virtuoso AMS Designer delivers the mixed-signal verification solution.

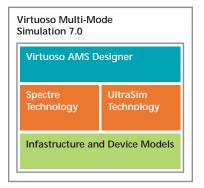


Figure 2: Virtuoso Multi-Mode Simulation

#### COMPREHENSIVE FEATURES

Spectre turbo technology specifically targets improving performance for transient analysis; however, all the production-proven capabilities of Spectre simulation are also supported. For example, Monte Carlo analysis will see similar speed-ups when the child analysis being run is a transient analysis.

All the advanced features of Spectre simulation are supported within the turbo technology release. For example:

- Assertions
- Verilog-A, MDL
- Statistical analyses, corners, and parametric sweeps

## USE MODEL

Spectre turbo technology enhances productivity further with its simple use model. With other performance enhancing approaches, customers can spend countless hours integrating and ramping up on new tools and capabilities—work that is often repeated for the next design or process node.

With Spectre turbo technology, the ramp-up time is zero. Designers only have to enable the turbo option—nothing changes in the netlist or model library—to take advantage of the turbo performance improvements. The following command line enables a Spectre "turbo" run:

#### % spectre +turbo ...

#### PARASITIC REDUCTION

Since parasitic reduction has an impact on accuracy and is applicable to a certain set of circuits, a separate command-line option enables it:

#### % spectre +turbo +parasitics ...

#### DESIGN ENVIRONMENT INTEGRATION

Spectre turbo technology integrates seamlessly within the Virtuoso Analog Design Environment, thus giving customers access to the performance boost through the GUI. Again, there is no rampup time required: all prior investment in a Spectre set-up is preserved and the turbo technology is easily enabled using a single option.

Spectre Turbo/Parasitic Reduction Options	
Turbo	⊻
Override Accuracy (Errpreset) Defaults	● Do not override  ⊖ Liberal  ⊖ Moderate  ⊖ Conservative
Multithreading options	🔾 Auto 🧶 Disable 👃 Manual
Number of threads	1
Parasitic Reduction	-
	OK Cancel Defaults Apply Help

Figure 3: Enabling Spectre turbo technology via the Virtuoso Analog Design Environment GUI

## **RETURN ON INVESTMENT**

Design teams and managers are constantly looking for advanced technologies to use in their custom IC development flow. The metrics they use to evaluate new tools are quality of results (QoR), use model, ease of adoption, and cost.

Spectre turbo technology addresses each one of these metrics. Designers can achieve the required performance improvement without sacrificing accuracy, while still maintaining the same use models they have today with Spectre Circuit Simulator.

## SUMMARY

With increasing design complexity, changing design metrics, shrinking process nodes, the requirements for high-performance and high-capacity analog simulation are clear.

Spectre turbo technology addresses these requirements with the same accuracy as the industry-standard Virtuoso Spectre Circuit Simulator, with significantly improved performance, greater productivity, and without disrupting the designer's environment and existing methodology.

For more information about this and other products contact: info@cadence.com or log on to: www.cadence.com

## cādence<sup>®</sup>

#### Cadence Design Systems, Inc.

#### CORPORATE HEADQUARTERS

2655 Seely Avenue San Jose, CA 95134 P:+1.800.746.6223 (within US) +1.408.943.1234 (outside US) F:+1.408.943.5001 www.cadence.com

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