

# VIRTUOSO

## Cadence Virtuoso Custom Design Platform





### PRECISELY THE FASTEST PATH TO DIFFERENTIATED SILICON

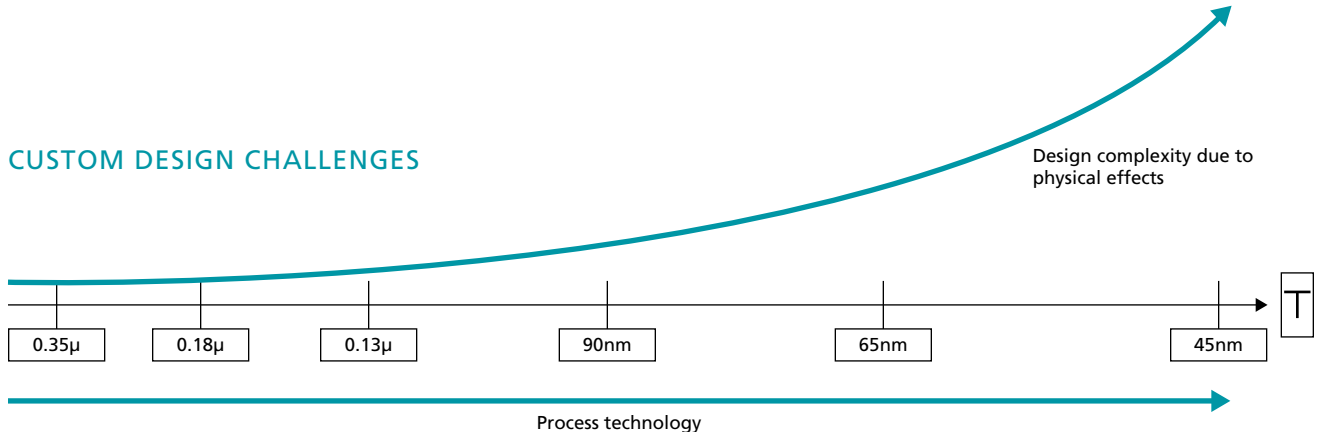
Personal consumer electronics and wireless products have become the dominant force in today's global electronics market. And relentless demand for new features and functionality in these devices is driving unprecedented growth in RF, analog, and mixed-signal applications. To create new products that fulfill this demand, IC designers must manipulate precise analog quantities—voltages, currents, charges, and continuous ratios of parameter values such as resistance and capacitance. This is when companies turn to custom design.

Full-custom design maximizes performance while minimizing area and power. However, it requires significant handcrafting by a select set of engineers with very high skill levels. In addition, custom analog circuits are more sensitive to physical effects, which are exacerbated at new, nanometer process nodes. To streamline the process of designing custom ICs and integrating them into end products, semiconductor and systems companies need sophisticated software and flow methodologies to meet time-to-market and time-to-volume goals.

The Cadence® Virtuoso® custom design platform accelerates the design of custom ICs across various process nodes. By selectively automating aspects of custom analog design and providing advanced technologies integrated on a common database, it allows engineers to focus on precision-crafting their designs—without sacrificing creativity to repetitive manual tasks.

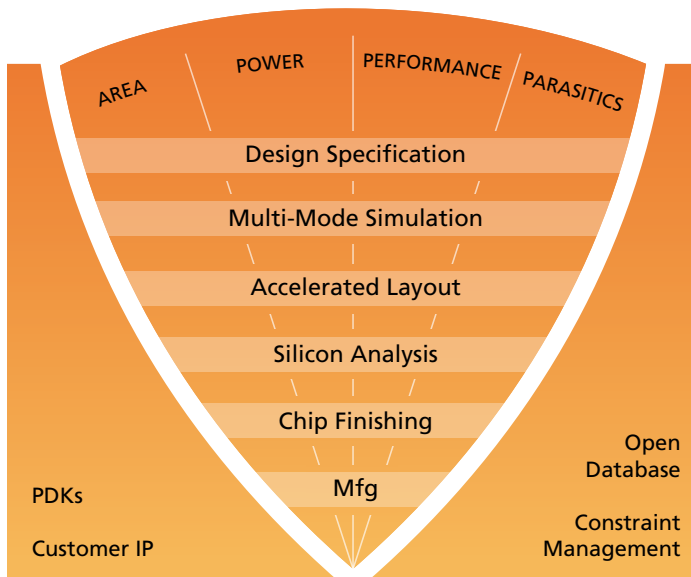
Cadence Design Systems is the global leader in software, hardware, methodologies and services that play essential roles in accelerating innovation in today's highly complex integrated circuits, printed-circuit boards, and electronics systems. Companies use Cadence® electronic design automation (EDA) technologies and engineering services to design, verify, and prepare advanced semiconductors and systems for manufacturing. These products in turn form the foundation of consumer electronics, networking and telecommunications equipment, and computer systems.

### CUSTOM DESIGN CHALLENGES



The Virtuoso platform addresses the increasing design challenges faced by electronics makers as they move to new process nodes

## THE VIRTUOSO CUSTOM DESIGN PLATFORM



All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

## A NEW APPROACH TO CUSTOM DESIGN

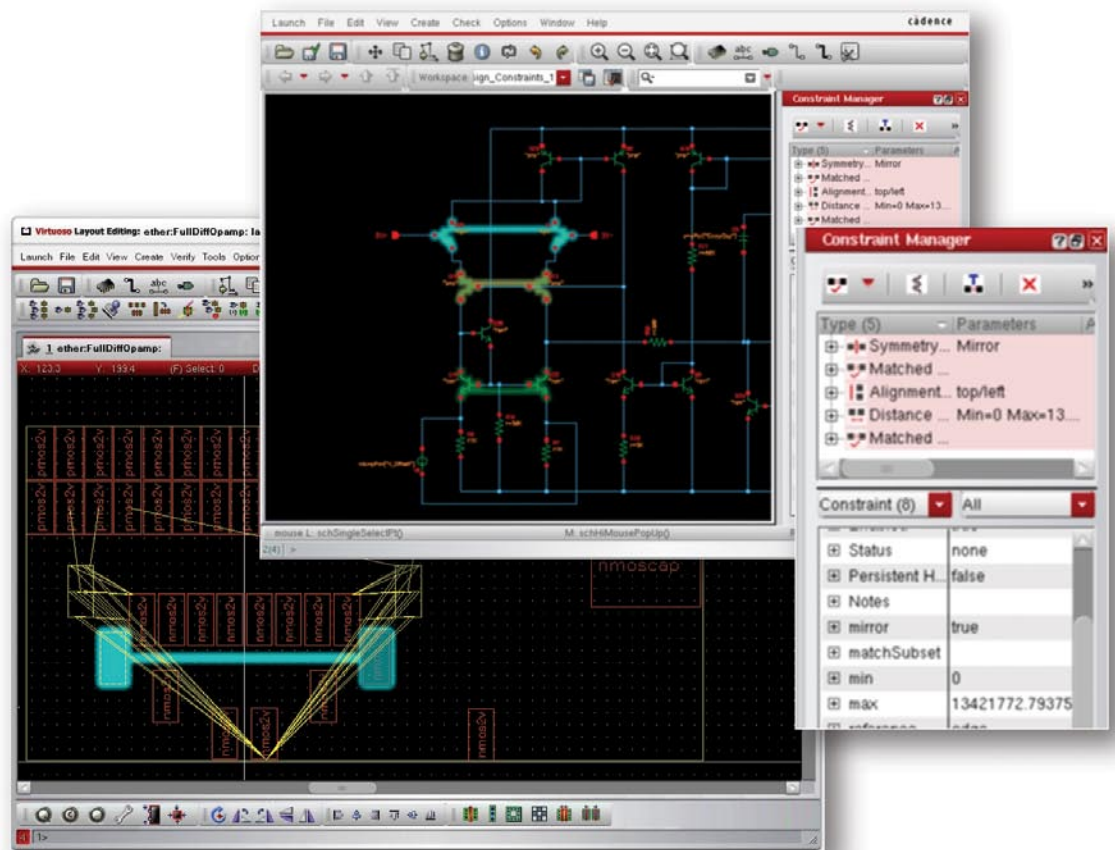
The Virtuoso custom design platform is a comprehensive system that accelerates the process of getting differentiated designs into silicon—at a variety of design nodes.

It includes advances like new constraint-driven design, which preserves design intent by enabling efficient design collaboration. Designers can specify design needs, save these constraints in context with the design, and then use this information to drive the accelerated layout solution to reduce errors.

Industry-leading high-speed simulators meet the stringent simulation and analysis requirements for analog, RF, and mixed-signal designs. Meanwhile, a new custom floorplanner allows analog design teams to rapidly explore multiple design architectures—and the implications of these design choices—prior to implementation.

Improved layout capabilities, a new user interface that greatly simplifies the complex tasks analog designers must perform, and integrated DFM further enhance the Virtuoso platform. The result is the fastest, most accurate path to the most differentiated silicon possible.

## AUTOMATED CONSTRAINT MANAGEMENT



A new unified constraint management system allows design teams to establish and share constraints across specification, simulation, and implementation

## SILICON ACCURACY

Virtuoso process design kits (PDKs) contain all the manufacturing-related parameters—from design rules to characterized models—needed to ensure a design will be manufacturable according to original design intent. At the heart of each PDK lies a silicon-calibrated device model. Virtuoso Multi-mode Simulation uses these same device models, therefore designs created using the Virtuoso platform achieve complete silicon accuracy. Virtuoso PDKs are available from Cadence as well as leading IC manufacturing companies such as TSMC, UMC, Chartered, IBM, and Jazz.

## ENHANCED DESIGN CAPTURE AND SIMULATION ENVIRONMENT

The Virtuoso design environment offers a variety of new methods to speed design creation and simulation. A revolutionary new way of working within the schematic editor allows engineers to use design constraints to more efficiently communicate with implementation engineers. This constraint-driven design approach lets designers specify design parameters—such as matching, symmetry, and alignment—and save these constraints in context with the design. They can use this information to drive an accelerated layout solution. The simulation environment then automatically captures the design process, such as the steps in the flow and the necessary data files, enabling designers to quickly build customized design methodologies. This method significantly boosts productivity, ensures consistency, and reduces errors.

The enhanced design environment also serves as a natural springboard to IP reuse. In addition, a parallel execution capability enables designers to quickly and easily characterize designs across all corners and statistical variations. It automates design reviews by instinctively generating reports that compare measured design data against specifications.

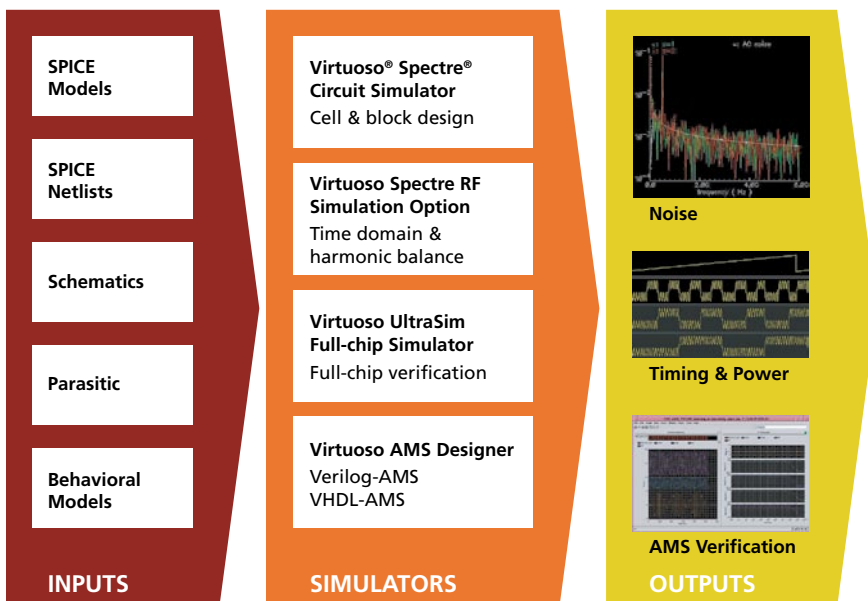
## WORLD-CLASS SIMULATION

Virtuoso Multi-mode Simulation provides custom IC designers with a complete design and verification solution for analog, RF, mixed-signal, memory and SoC designs. Virtuoso Multi-mode Simulation is a combination of the industry's leading SPICE, Fast SPICE, RF, and analog mixed-signal simulators in a unique shared licensing package. It is designed to meet the changing simulation needs of designers as they move through the design cycle—from architecture exploration to block level development to RF design and to final full-chip verification. Customers can choose the right simulator for the job. These include Virtuoso Spectre® Circuit Simulator, Virtuoso Spectre RF Simulator, Virtuoso UltraSim Full-Chip Simulator, and Virtuoso AMS Spectre and Virtuoso AMS Ultra options.

## ACCELERATED LAYOUT

Virtuoso accelerated layout provides the fastest path to custom physical design. It delivers an unparalleled set of features—from QuickCell parameterized cell definition to design rule-driven support. More advanced capabilities such as constraint-based connectivity-driven design, floorplanning, and design optimization further help to achieve better yield. Connectivity-driven layout provides a proven 4-10x productivity boost over manual layout editing, while design rule-driven support ensures correct-by-construction layout, which is especially important at advanced design geometries. Also included are automated custom placement and automated custom routing capabilities, which not only follow the technology file but also the design constraints entered by the front-end designer. For users who prefer fully automated layout of blocks, Virtuoso accelerated layout also supports constraint-based layout synthesis.

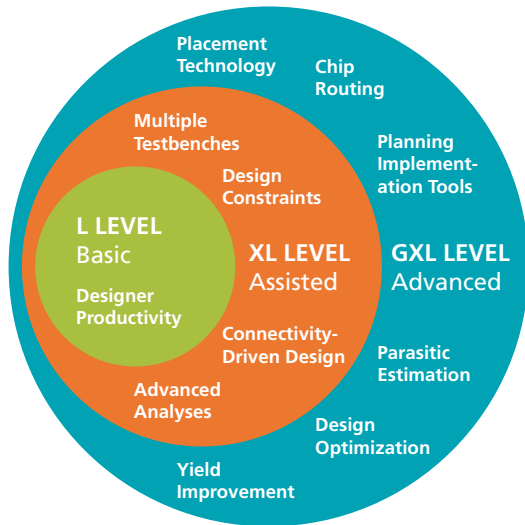
## VIRTUOSO MULTI-MODE SIMULATION



Four industry-leading simulation engines use a common syntax, equations and models to solve analog, RF, AMS, memory, and full-chip simulation needs



## FLEXIBLE PRODUCT CONFIGURATIONS



The Virtuoso platform comes configured in three versions, each designed to meet specific needs

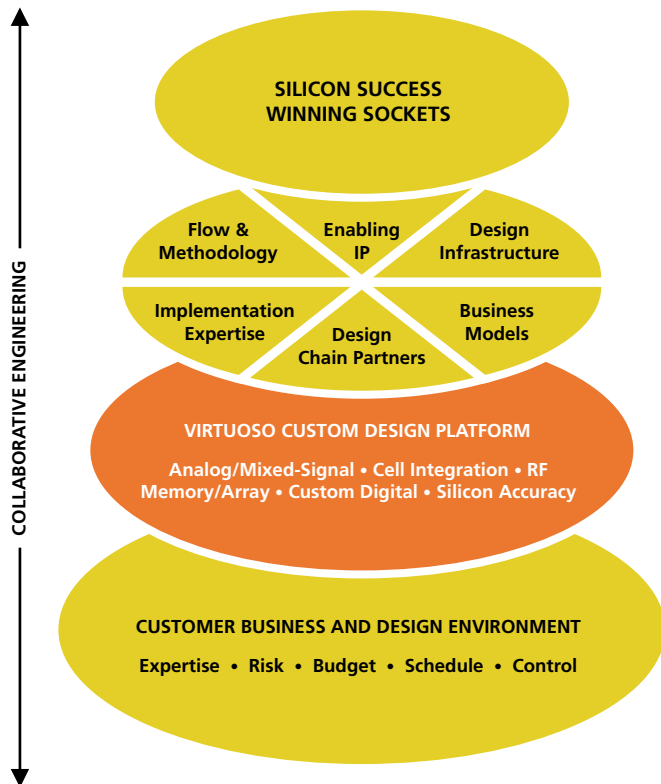
## SILICON-ACCURATE ANALYSIS

For analog/mixed-signal design at 0.18 micron and below, high-accuracy parasitic extraction, analog IR-drop analysis, and power grid electromigration analysis become critical for both circuit design and full-chip electrical verification. Virtuoso silicon analysis combines all of these capabilities with design rule checking (DRC) and layout-versus-schematic checking (LVS). For high-frequency designs (>1GHz), Virtuoso silicon analysis includes inductance extraction, signal-wire electromigration analysis, and a fast field solver for capacitance extraction. These capabilities enable design teams to perform silicon-accurate analysis quickly and avoid extremely expensive unplanned re-spins.

## COMPREHENSIVE DESIGN FINISHING TECHNOLOGIES

Several sophisticated Virtuoso technologies address the most demanding design finishing tasks. Because the Virtuoso platform is built on OpenAccess, design teams can pass designs back and forth freely between custom and cell-based environments without using translators. Virtuoso chip finishing technologies include the world's most advanced chip-level routing for 90nm and 65nm designs, a new and industry-proven chip optimization technology for optimizing design routes at the top-level, and migration technologies to ease the reuse of custom digital IP. Nonetheless, design finishing involves more than just physical design; it also requires silicon analysis, such as IR-drop, and substrate noise analysis capabilities that are required for advanced process technologies. The Virtuoso platform offers the industry's most complete set of full-chip silicon analysis capabilities.

## PARTNERING THROUGH PRODUCTION



Silicon success requires much more than a fast, silicon-accurate design platform. It requires flows, expertise, IP, and partnerships optimized for specific designs, budgets, and schedules.

By offering a collaborative engineering approach, Cadence Engineering Services can become an extension of your team

## VIRTUOSO PLATFORM CONFIGURATIONS—DESIGNED FOR FLEXIBILITY

Cadence offers the Virtuoso custom design platform as tiered families of products. Each configuration provides a set of capabilities tailored to different needs. The L family is an entry-level version, providing the proven capabilities of this industry-leading custom IC design environment. The Virtuoso custom design platform XL family of products extends the L family to provide higher levels of design assistance to the end user, including new design constraints, correct-by-design layout, and advanced simulation modes. The GXL family further delivers the platform's most advanced capabilities, including design optimization for yield, cell and floor planning capabilities, and sophisticated routing technology.

For more information about the Virtuoso platform, log on to [www.cadence.com/virtuoso](http://www.cadence.com/virtuoso)

## GLOBAL LOCATIONS

### Asia Pacific

Beijing, China  
Chengdu, China  
Hsinchu, Taiwan  
Hong Kong, China  
Seoul, Korea  
Shanghai, China  
Shenzhen, China  
Singapore  
Taipei, Taiwan

### India

Bangalore  
New Delhi

### Japan

Shin-Yokohama

### EMEA

Bracknell, England  
Feldkirchen, Germany  
Herzlia, Israel  
Meylan Cedex, France  
Milan, Italy  
Paris, France  
Sophia Antipolis, France  
Stockholm, Sweden

### North America

Arden Hills, Minnesota  
Austin, Texas  
Bellevue, Washington  
Blue Bell, Pennsylvania  
Chelmsford, Massachusetts  
Columbia, Maryland  
Irvine, California  
Louisville, Colorado  
Ottawa, Canada  
Ontario, Canada  
Plano, Texas  
San Diego, California  
San Jose, California  
Schaumburg, Illinois  
Tempe, Arizona  
Tigard, Oregon  
Tinton Falls, New Jersey

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