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Cadence NanoRoute Advanced Digital Router

Concurrent timing, area, signal integrity, and manufacturing convergence for 100M+ instance designs

Cadence® NanoRoute® Advanced Digital Router is the industry-leading unified routing and interconnect optimization solution that helps you quickly achieve concurrent timing, area, signal integrity, and manufacturability convergence during digital implementation. Integrated with Cadence Encounter® Digital Implementation System and available as a standalone router, the NanoRoute solution ensures top-quality silicon for high-performance designs using both advanced or mainstream process technologies.

Overview

Advanced process node designs require a new generation of physical-, electrical-, and manufacturing-aware routing technology. In all designs today, power and manufacturability issues are enormous and interdependent with timing, signal integrity, and area requirements. In addition, 20/16/14nm advanced node processes create new considerations in the form of double patterning and FinFET device usage, requiring the router to balance multiple design objectives concurrently while mitigating on-the-fly any potential risks to performance and yield. Last, but not least, a viable router must have the speed to meet aggressive time-to-market schedules.

NanoRoute Advanced Digital Router handles all routing challenges at both block and full-chip levels. It combines the performance characteristics of a grid-based router with off-grid flexibility, and it simultaneously evaluates and optimizes interconnect topology based on the 3D effects on timing, area, power, manufacturability, and yield. Powered by a super-threading backplane (multi-threaded and distributed

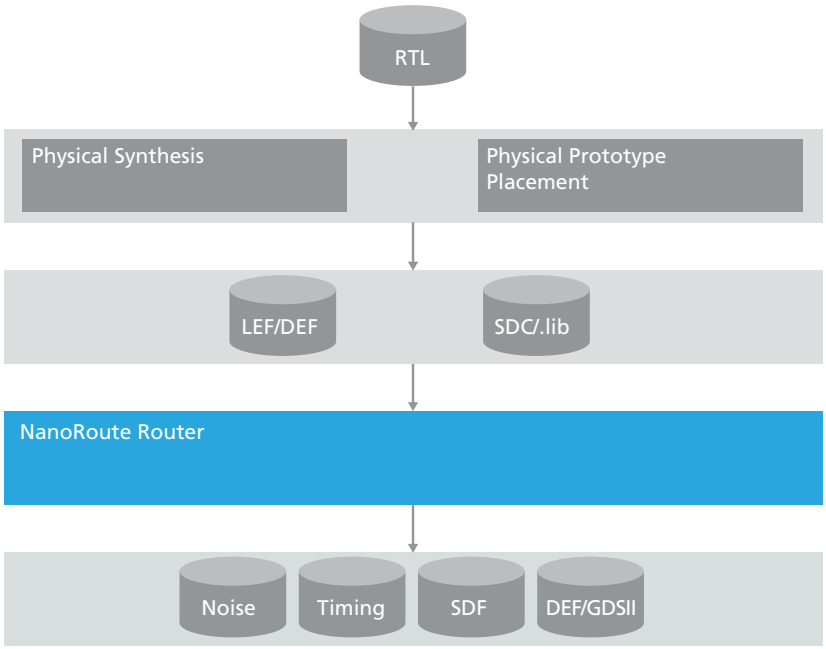

Figure 1: NanoRoute Advanced Digital Router integrates with Encounter Digital Implementation System, but is also available as a standalone product

processing combined), the NanoRoute solution finishes millions of nets of connectivity per hour. It delivers the highest quality of results in a fraction of the time taken by other routers on the market. NanoRoute technology is also fully equipped to handle 20/16/14nm design requirements, including double patterning and FinFET support. Using a correct-by-construction approach, the NanoRoute Router resolves potential double-patterning conflicts on-the-fly for a routing topology that is not only double patterning- and advanced DRC-correct the first time, but is also more area efficient.

Benefits

Fully certified/qualified by foundries to support the latest 20/16/14nm process rules

- Ensures design and routing convergence for designs integrated with advanced process technologies
- Supports correct-by-construction double patterning with FlexColor routing technology

Enables the implementation of high-performance designs on advanced or mainstream process technologies

- Mitigates process variation by supporting a wide range of advanced node processes
- Improves overall quality of results, maximizes utilization, and meets multiple design objectives
- Shrinks die size by 5-10% with robust routing technology and congestion handling results
- Offers higher capacity for larger, more complex designs

Enhances productivity through efficient single-CPU and multi-CPU performance

- Delivers 10x or more performance gain using super-threading technology
- Speeds turnaround time with dynamic multi-thread and distributed processing capability

Ensures a smooth path to design tapeout and production silicon

- Offers a silicon-proven track record with successful customer tapeouts and foundry endorsements

Features

Smart routing

NanoRoute Advanced Digital Router features a new generation of **SMART** technology, **SMART2**, which simultaneously evaluates and optimizes the interdependent objectives of signal integrity, manufacturing awareness, routing, and timing for faster design convergence—all while preserving design intent. **SMART2** technology offers:

- Full support of process design rules (both restricted and recommended) from 130nm to 20/16/14nm and smaller
- Design for manufacturability capabilities such as via and interconnect optimization
- Correct-by-construction double-patterning routing, and automated prevention and fixing for lithography effects

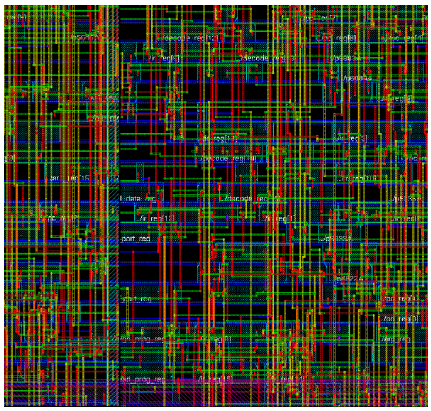

Figure 2: **SMART2** *technology targets multiple design objectives simultaneously for total design closure*

- Shielding support and signal integrity 3D coupling effect reduction
- Large capacity and high utilization support
- Dynamic multi-CPU support with super-threading technology

In traditional approaches to routing, issues such as coupling effect, power, area, and especially design for manufacturing (DFM) are addressed sequentially and in a manner that is mutually exclusive from one another. But signal integrity and power are isolated from process variation and should not be optimized separately from manufacturability. A fix for one requirement will likely introduce a change for the other and create new conflicts. The same is true for routability and manufacturing awareness. New foundry-enforced manufacturing requirements such as double patterning requirements, DRC rules to support FinFET devices, and yield enhancement guidelines can significantly alter the RC characteristics and cross coupling dynamics of the design. Changes to either must be aware of both timing and signal integrity. By using the **SMART2** approach to routing—concurrent optimization with in-context analysis—design teams can intelligently manage all design objectives simultaneously. Key capabilities include:

- Wire spreading
- Wire widening
- Double cut via insertion
- Single-via reduction and optimization
- Critical area analysis and optimization
- True lithography distortion prevention and optimization
- CMP-aware metal fill
- And a rich set of random and systematic visual analysis and text-based reporting vehicles

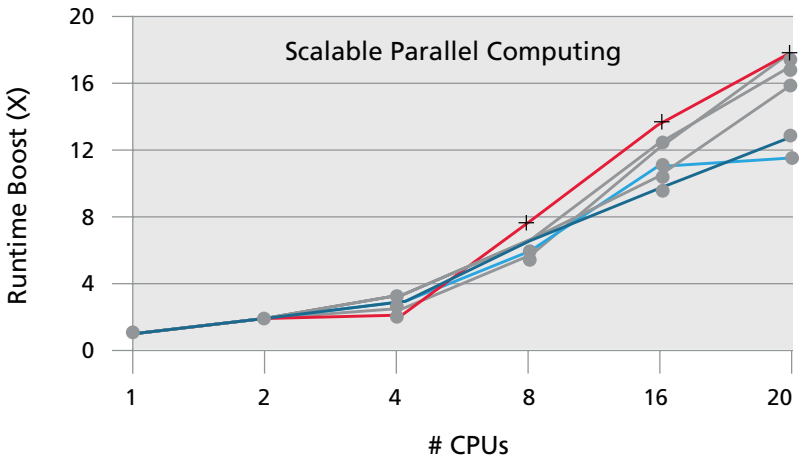

Figure 3: Performance scales linearly with the number of CPUs used

Scalable performance and capacity

Maximizing performance and minimizing memory footprint on a single CPU, the advanced NanoRoute super-threading architecture delivers linearly scalable turnaround time on a multi-thread platform or distributed CPU configuration. Its dynamic resource allocation across a heterogeneous HW/SW network environment or compute farm instantly makes use of available resources without sitting in network traffic congestion.

Flow support

NanoRoute Advanced Digital Router provides standard interfaces to common industry design and verification methodologies to support plug-in flows:

- Integrates easily with any production design flow
- Supports industry-standard design constraints, libraries, and data formats
- Provides an OpenAccess interface for interoperability between multidisciplinary design environments
- Provides a Tcl/Tk programming interface for database access, scripting, and design environment customization

Platforms

- Sun Solaris (32- and 64-bit)
- HP-UX (32- and 64-bit)
- Linux (32- and 64-bit) [Opteron and Itanium]

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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