DATASHEET

VIRTUOSO CHIP ASSEMBLY ROUTER

The Cadence® Virtuoso® Chip Assembly Router is the custom IC transistor, cell, block, and advanced chip-level interconnect technology in the Virtuoso custom design platform. The Virtuoso Chip Assembly Router is a constraint- and design-rule-driven, interactive, and fully automatic shape-based router. It supports both block authoring and chip authoring solutions for custom digital, mixed-signal, and analog designs at any level of the hierarchy.

THE VIRTUOSO CUSTOM DESIGN PLATFORM

When design objectives dictate manipulating precise analog quantities—voltages, currents, charges, and continuous ratios of parameter values such as resistance and capacitance—companies turn to custom design. Full-custom design maximizes performance while minimizing area and power. However, it requires significant handcrafting by a select set of engineers with very high skill levels. In addition, custom analog circuits are more sensitive to physical effects, which are exacerbated at new, nanometer process nodes.

The Virtuoso custom design platform accelerates the design of custom ICs across various process nodes. By selectively automating aspects of custom analog design and providing advanced technologies integrated on a common database, it allows engineers to focus on precision crafting their designs—without sacrificing creativity to repetitive manual tasks.

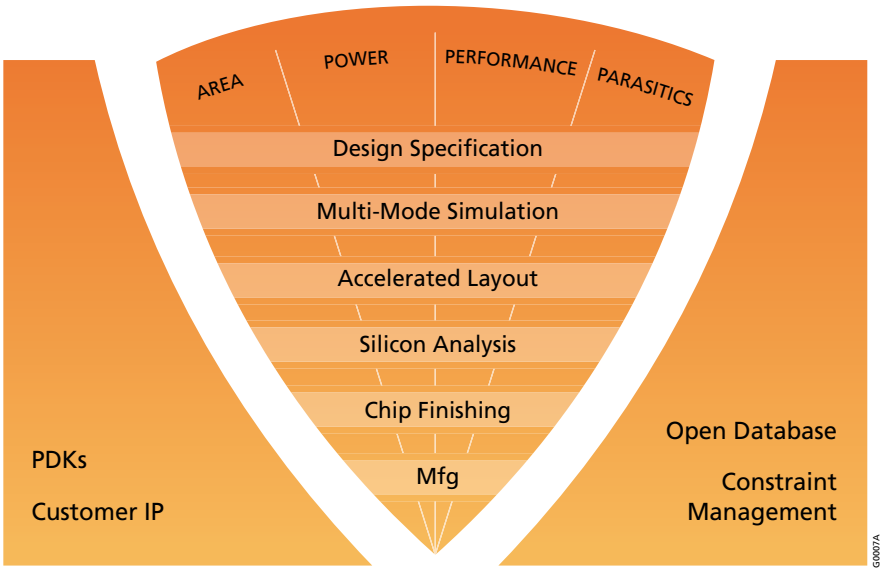

Figure 1: All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

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VIRTUOSO CHIP ASSEMBLY ROUTER

The Virtuoso Chip Assembly Router is a design constraint- and process rule-driven, interactive, and fully automatic shape-based gridless router that supports transistor, cell, block and chip-level routing for custom digital, mixed-signal, and analog designs at any level of the design hierarchy. The Virtuoso Chip Assembly Router is interoperable with both the Virtuoso custom design platform and the Cadence Encounter® digital IC design platform. A unique blend of interactive and automatic design constraint- and process rule-driven routing features are provided, simplifying the most complex interconnect issues and maximizing productivity. The Virtuoso Chip Assembly Router supports 90nm and above process technology rules and is available on OpenAccess.

BENEFITS

- Increased productivity and design quality through the specification and adherence of complex constraint and process rules during interactive and automatic routing
- Simplified routing process using advanced features such as interactive push and shove, multi-net/bus, power, shielding, differential pairs, length, and crosstalk (*see Figure 2*)
- Intuitive, easy-to-use interface with menu, command, and 'do' file use options
- Open and flexible interoperability with the Virtuoso Schematic Editor and Virtuoso XL Layout Editor to support dynamic cross-probing and editing (*see Figure 3*). Interoperability with the SoC Encounter™ system is also supported

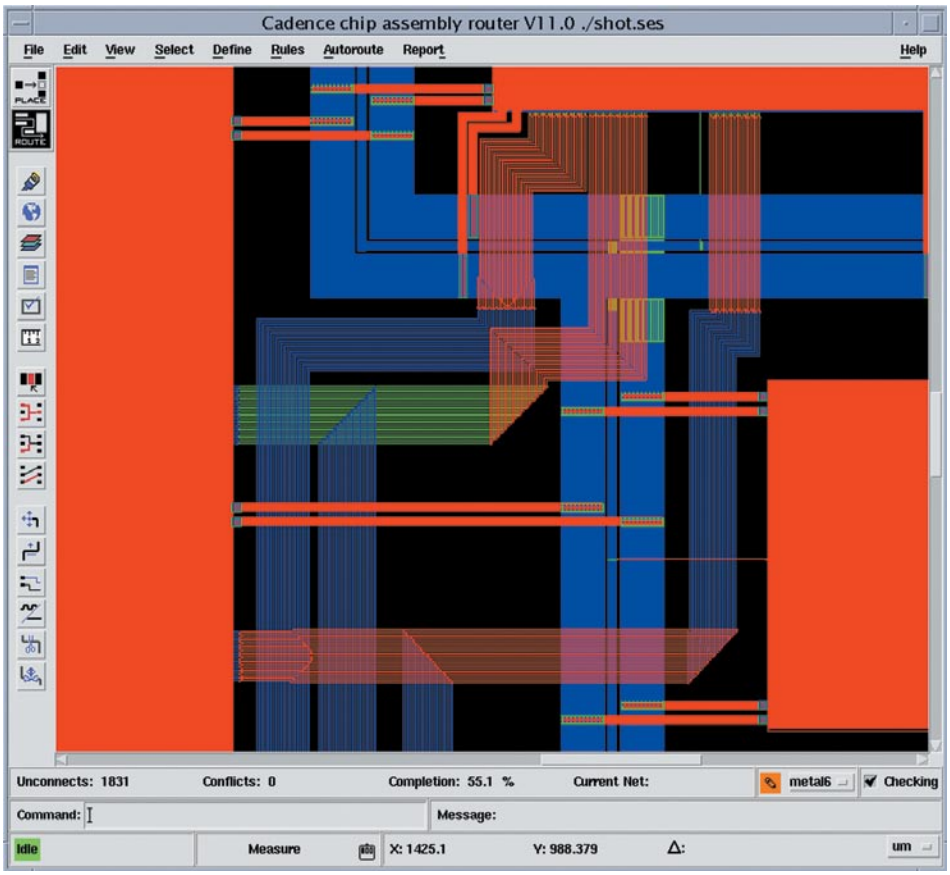

Figure 2: Interactive and automatic bus and power routing

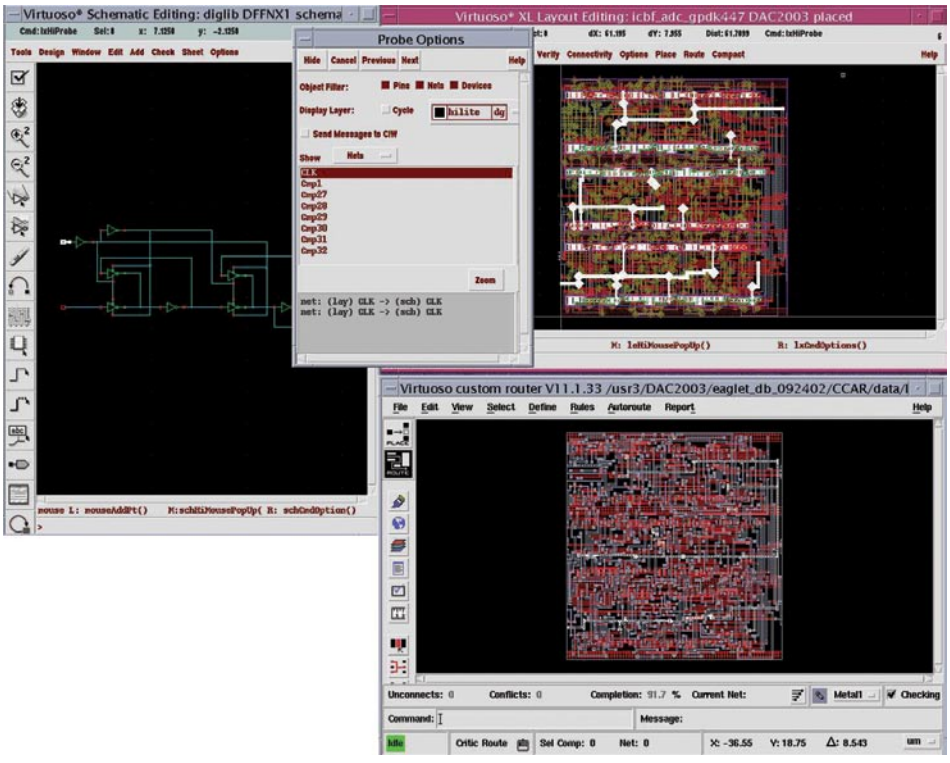

Figure 3: Real-time interoperability with the Virtuoso Schematic Editor and the Virtuoso XL Layout Editor to provide accurate and accelerated block and chip design

FEATURES

DESIGN CONSTRAINT AND PROCESS RULE-DRIVEN ROUTING

The Virtuoso Chip Assembly Router accelerates the design process by providing a comprehensive set of design constraints and process rules that are specified, managed, and obeyed in a hierarchical precedence order during interactive and automatic routing. Dynamic real-time checking is performed during interactive routing with a halo display and automatic enforcement of the rules (*see Figure 4*). Automatic routing rules are obeyed during routing with optional post-route checking of the entire design or selective areas of the design.

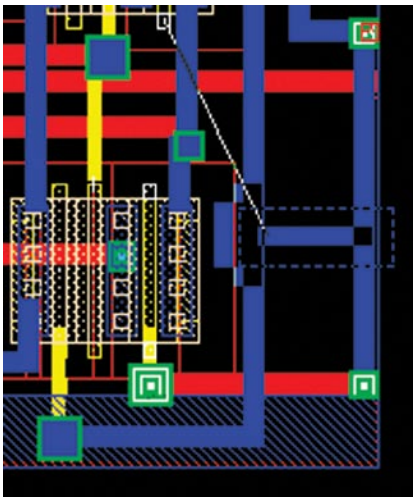

Figure 4: Interactive routing uses connectivity-, constraint-, and design-rule–driven features with push and shove for fast and accurate editing

ADVANCED INTERACTIVE ROUTING FEATURES

The Virtuoso Chip Assembly Router simplifies the routing process with advanced interactive and automatic routing features. Interactive routing provides push and shove routing that eliminates the need to move other adjacent routing obstructions. Multi-net/bus routing supports the routing of two or more nets to efficiently route large bus structures. Power is fully automated with pin-to-trunk, cell row, block ring, I/O ring, and stripes/mesh features.

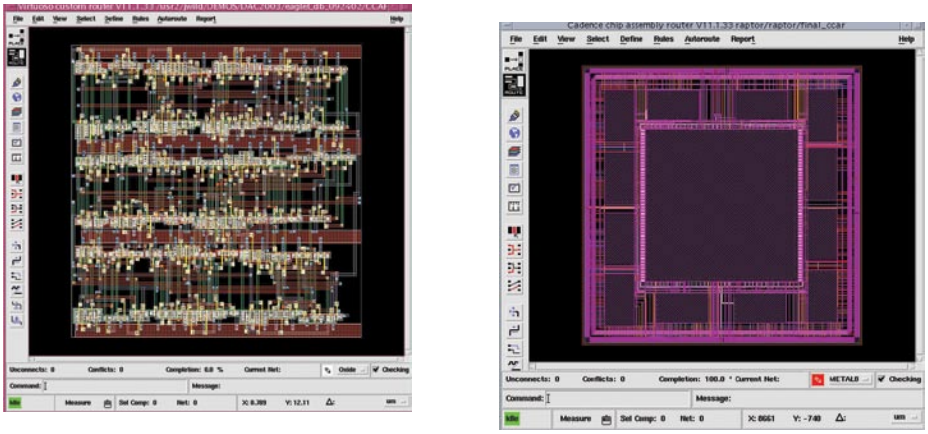

Figure 5: Interactive/automatic routing for analog, mixed-signal, and custom digital designs at the device, cell, block, and top levels

FLEXIBLE SUPPORT CUSTOM BLOCK AND CHIP ROUTING

The Virtuoso Chip Assembly Router simplifies the adoption and implementation of its unique custom block and chip routing solution with an intuitive and easy-to-use interface. It dynamically interoperates with Virtuoso Schematic E0ditor schematics and Virtuoso XL Layout Editor layouts, with cross-probing of instances and nets in addition to dynamic editing changes. Virtuoso XL Layout Editor compatibility features are provided to map mouse and keyboard binding, selection, zoom, and panning functions from Virtuoso XL Layout Editor to Virtuoso Chip Assembly Router. The Virtuoso Chip Assembly Router is interoperable with Virtuoso Chip Editor and SoC Encounter digital floorplanning and routing tools. It is also interoperable through LEF/DEF and the OpenAccess database.

SPECIFICATIONS

INTERACTIVE AND AUTOMATIC ROUTING

- Variable width and spacing rules
- Antennae rule checking and fixing
- 90nm process rule support (via adjacency, width-based, proximity, and maximum width)
- Advanced interactive routing with push and shove, automatic completion, and route-to-cursor
- Automatic global, track, and detail routing
- Congestion analysis and automatic channel sizing
- Device-, cell-, block-, and top-level chip assembly routing support (*see Figure 5*)
- ECO functions
- Design and rule reporting
- Automatic power routing (pin-to-trunk, cell row, block ring, I/O ring, and stripes/mesh)
- Pre-route pin checking to insure routability
- Incremental design and selective net routing
- Polygon editor
- Topology editor
- Automatic specialty routing support for shielding, differential pairs, and symmetry (*see Figure 6*)
- Net length control including minimum, maximum, and matched
- Multiple via, via array, and minimum area via support
- Pin width matching and tapering
- Manufacturing and yield enhancement post-processing

DESIGN INPUTS

- Cadence CDBA database
- OpenAccess database
- LEF/DEF format
- STREAM format
- EDIF

DESIGN OUTPUTS

- Cadence CDBA database
- OpenAccess design data
- DEF format
- STREAM format

PLATFORM/OS

- Sun/Solaris
- HP-UX
- IBM AIX
- Linux

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
  - Collaborative approach and design infrastructure—virtual teaming
  - Proven methodology and flow tuned to your design environment
  - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
  - Over 80 instructor-led courses—certified instructors, real world experience
  - More than 25 Internet Learning Series (iLS) online courses
- Cadence customer support that keeps your design team productive
  - Cadence applications engineers provide technical assistance
  - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

For more information
Email us at **info@cadence.com**
or log on to **www.cadence.com**

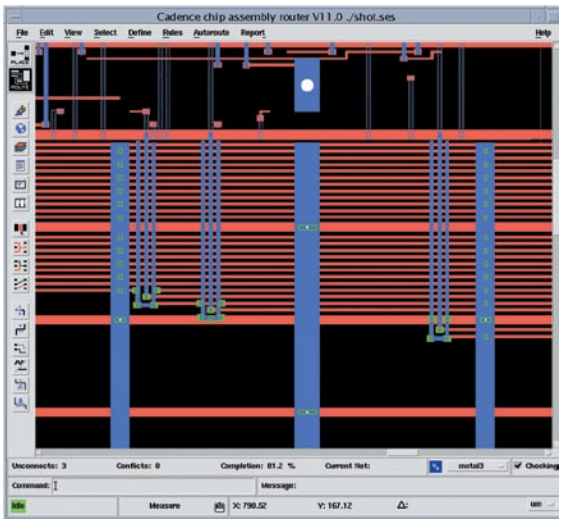

Figure 6: Analog, mixed-signal routing features—auto net shielding

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