DATASHEET

VIRTUOSO ANALOG ELECTRONSTORM OPTION

The Cadence® Virtuoso® Analog ElectronStorm® Option adds signal electromigration to the Virtuoso custom design platform. This option to the Virtuoso Analog Design Environment addresses electromigration validation for analog designs, which is especially important because signal electromigration is an increasing concern for analog designers using high-powered transistors or advanced process technologies.

THE VIRTUOSO CUSTOM DESIGN PLATFORM

When design objectives dictate manipulating precise analog quantities—voltages, currents, charges, and continuous ratios of parameter values such as resistance and capacitance—companies turn to custom design. Full-custom design maximizes performance while minimizing area and power. However, it requires significant handcrafting by a select set of engineers with very high skill levels. In addition, custom analog circuits are more sensitive to physical effects, which are exacerbated at new, nanometer process nodes.

The Virtuoso custom design platform accelerates the design of custom ICs across various process nodes. By selectively automating aspects of custom analog design and providing advanced technologies integrated on a common database, it allows engineers to focus on precision crafting their designs—without sacrificing creativity to repetitive manual tasks.

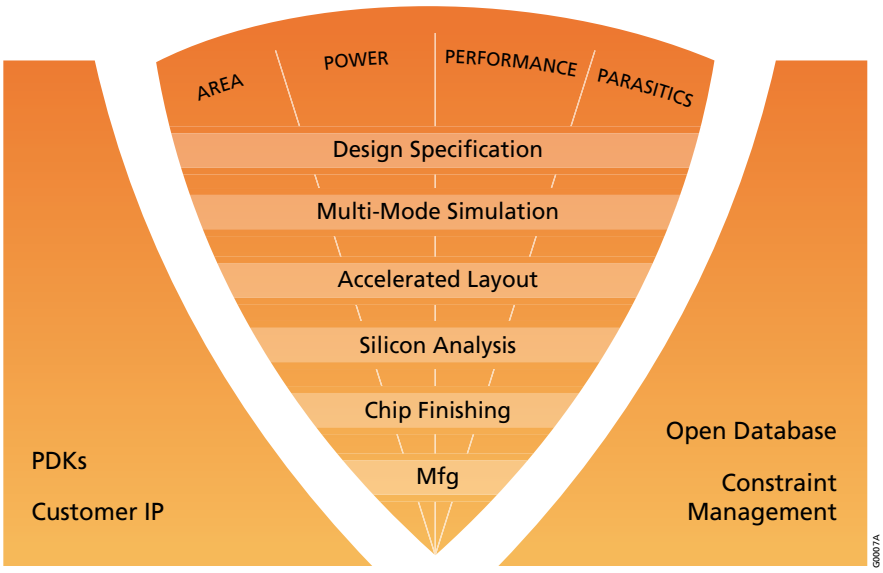

Figure 1: All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

cadence™

VIRTUOSO ANALOG ELECTRONSTORM OPTION

Integrated tightly with the Virtuoso Analog Design Environment design creation product, the option performs signal electromigration verification for analog and mixed-signal designs. It works with Assura® LVS, Assura RCX, and Virtuoso Spectre® Circuit Simulator to perform a full-chip circuit simulation specifically targeted for signal electromigration verification. Signal electromigration is comprehensively checked for all interconnect segments and vias within the net, and you can optionally include power rail IR drop in the simulation for even more accuracy. Thermal plots of signal electromigration are directly displayed in the Virtuoso Analog Design Environment GUI, where you can easily address any identified issues or problems. The thermal plots are supported by a full textual report which contains details of the analysis results.

BENEFITS

- Reduces risk of tapeout failure due to signal electromigration
- Reduces risk of expensive field-failures—higher quality designs
- Maximizes user efficiency by displaying signal electromigration results directly on the circuit layout
- Extends the value of existing extraction and simulation product
- Includes an easy-to-use menu-based interface to Virtuoso Analog Design Environment

FEATURES

TIGHT INTEGRATION WITHIN VIRTUOSO ANALOG DESIGN ENVIRONMENT

Virtuoso Analog Design Environment is the market-leading solution for analog design creation. The option extends the value of Virtuoso Analog Design Environment by adding signal electromigration verification, necessary for most of today's complex designs. Using an additional pull-down menu option within the Virtuoso Analog Design Environment menu bar, signal electromigration can be rapidly analyzed using user-provided simulation vectors. Results of the analysis are displayed directly on the layout within the Virtuoso Analog Design Environment GUI, which enables easy debugging of any signal electromigration issues. An easy-to-use pop-up form displays the textual analysis results which can also be used to drive the debugging activity.

ACCURATE ELECTROMIGRATION ANALYSIS

Copper process technologies complicate electromigration analysis because current density limits vary with the width of the metal interconnect. The ElectronStorm option enables you to enter multiple current density limits per interconnect layer, to allow you to accurately set the electromigration limits. The temperature for the analysis is also user-definable, and a temperature scaling factor enables you to execute electromigration analysis at one temperature and scale the results for temperature corners using foundry-supplied factors *(see Figure 2).*

STANDARD PRODUCT UTILIZATION

The Virtuoso Analog ElectronStorm Option uses the most common parasitic extraction and circuit simulation tools within the Virtuoso Analog Design Environment, namely Assura LVS, Assura RCX, and Virtuoso Spectre simulation. This enables you to rapidly ramp up signal electromigration verification by using your existing control decks for these products, without having to learn new extraction or simulation engines.

DYNAMIC SIMULATION APPROACH

Since the signal electromigration solution executes a complete circuit simulation (optionally including the impact of IR drop on both power and ground rails), it increases confidence that your design will function correctly on silicon. For the highest confidence, signal electromigration should be validated at worst-case process corners.

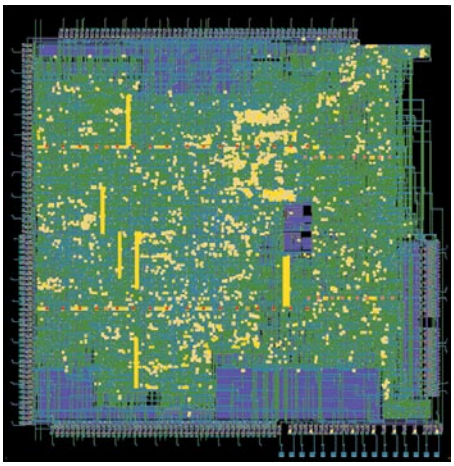

Figure 2: Signal filtering for electromigration (SIFT-EM) technology applies EM risk analysis to clock and signal nets

SPECIFICATIONS

EASY SETUP

- Form-based setup for signal electromigration verification
- Supports via and wire electromigration limits
- Electromigration limits set per layer and per width

SIGNAL ELECTROMIGRATION RESULTS

- Form-based reporting of electromigration results
  - Clear identification of failures
  - Clear identification of required sizes to fix violations
  - Ordered listing (worst violators listed first)
- Reports RMS, maximum, or average results
- Goto next error capability for easy debug
- Temperature scaling factor adjusts results based on new temperature *(see Figure 3)*

PLATFORM/OS

- Sun/Solaris
- HP-UX
- Linux

CAPACITY

- 50,000 transistors
- 500K parasitic resistors

Figure 3: The option highlights the locations in signal lines that are subject to Joule heating failures

ASSOCIATED PRODUCTS

ASSURA DRC/LVS

- Tight integration with Virtuoso Layout Editor and Virtuoso Schematic Editor
- Full-featured batch and interactive verification tool
- Fast verification runtimes for highly repetitive and hierarchical designs
- Correctly verifies design connectivity regardless of layout methodology or hierarchy
- Automatically extracts devices formed across layout hierarchy
- Significantly reduces runtimes using multi-processing for device extraction
- Complete flexibility through user-defined device parameters and user-programmable rule files
- Supports all designs—analog, digital, RF, SiGe, and SOI designs

ASSURA RCX

- Accurate interconnect parasitic extraction
- Reduces cost-of-ownership with easy adoption into existing production flows
- Seamless integration with Virtuoso Analog Design Environment
- Supports industry-leading Si (0.13µm and below) and SiGe process technologies
- Advanced 3-D modeling capabilities
- Supports local interconnect, air gaps, conformal and multiple dielectric, copper effects

VIRTUOSO SPECTRE CIRCUIT SIMULATION

- Full integration with Virtuoso AMS Designer, Cadence Design Framework II, Incisive® Unified Simulator, and Virtuoso Analog Design Environment
- Advanced architecture supports large circuits containing more than 50,000 transistors
- Fully-integrated analog hardware description languages (AHDL) extend modeling capabilities, boosts simulation performance, and supports top-down design styles for rapid development of complex circuits and testbenches
- Comprehensive semiconductor model support combined with industry-leading foundry models
- Versatile analysis capability leads to increased designer confidence
- Superior simulation accuracy and performance for tough analog and mixed-signal circuits

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
  - Collaborative approach and design infrastructure—virtual teaming
  - Proven methodology and flow tuned to your design environment
  - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
  - Over 80 instructor-led courses—certified instructors, real world experience
  - More than 25 Internet Learning Series (iLS) online courses
- Cadence customer support that keeps your design team productive
  - Cadence applications engineers provide technical assistance
  - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

For more information

Email us at info@cadence.com

or log on to www.cadence.com

cadence™

Cadence Design Systems, Inc.

2655 Seely Avenue
San Jose, CA 95134
P:+1.800.746.6223 *(within US)*
+1.408.943.1234 *(outside US)*
www.cadence.com

© 2007 Cadence Design Systems, Inc. All rights reserved. Cadence, Assura, ElectronStorm, Incisive, Spectre, SourceLink, and Virtuoso are registered trademarks and the Cadence logo is a registered trademark of Cadence Design Systems, Inc. All others are properties of their respective holders.

7097B 02/07